By using Synopsys' ASIP Designer tool, we were able to reduce gate count by 70%, which enabled us to implement our design in an FPGA and retain the required system performance of printing 70 pages a minute with our multifunction printer."

Manager, Controller Development Group, Fuji Xerox

Fuji Xerox's full-color digital multifunction printer
[illegible] instruction-set processor (ASIP) approach and selected Synopsys' ASIP Designer tool.

[illegible] printer

Reduce system development cost

Flexibility to avoid design respins

[illegible] instruction set processors (ASIPs)

Explored and optimized processor architecture to reduce area and system development cost

Reduced gate count by 70% compared to fixed-function hardware accelerators

Rapid architectural exploration using compiler-in-the-loop technology

Automatic generation of a fully featured software development kit (SDK) including an optimizing C compiler

No royalty costs

In contrast to standard fixed-function hardware accelerators, ASIPs enable the design of very efficient accelerators that are controlled by application-specific instructions rather than by a state machine. Due to its specialization, ASIPs can match the performance of fixed RTL designs and, by applying resource sharing, can result in smaller area. An ASIP is fully software programmable, so the algorithm can be changed even after tapeout.

Fuji Xerox selected Synopsys' ASIP Designer, the industry's leading ASIP design tool environment. ASIP Designer uses a single input specification to generate a software development kit (SDK) featuring a highly optimizing C compiler, instruction-set simulator (ISS), assembler, linker and debugger, as well as the synthesizable RTL. The generated ISS, including its advanced profiling capabilities, and the unique compiler-in-the-loop technology, allowed for rapid architectural exploration, as Fuji Xerox was able to profile the architecture against their algorithms right away. ASIP Designer's nML processor modeling language enabled the design team at Fuji Xerox to make rapid changes in the processor model, which were then reflected in RTL, C compiler, and simulator, making it easy to make iterative enhancements to the processor.

As pres pp 2.9(e)-6.7(s [illegible]J0 Tc 0 T)4.[illegible](a)9.1(t)2[illegible](e)-[illegible]5(d)11([illegible]J0 -1

"Synopsys' ASIP Designer provided us with the ability to start software development early and efficiently conduct architectural exploration and optimization of the design, saving a lot of time and freeing the development team to focus on other aspects of the project."

Manager, Controller Development Group, Fuji Xerox