Synopsys XHF OTP NVM IP

Highlights

- Memory capacity: 16 Kbits to 128 Kbits
- Output data bus: 32 bits, 48 bits if not using reliability and special security features of the OTP
- Dual power supply: VDD and VDDIO
- IPS supporting single-bit programming both in the factory and field
- Minimum data retention of 10 years
- Standardized APB Interfaces to ease design integration
- Low power mode
- Robust design with error correction code (ECC) and repair bits
- 10x faster programming time for test cost reduction
- OTP controller to support built-in-self-test (BIST), programming, ECC, and repair
- Word-level read-and-write locks
- Macro-level read and write locks
- Security features including dedicated APB interface for testing and programming, safe boot, and OTP wipeout feature

Target Applications

- Trim settings and calibration
- ROM and eFuse replacement
- Encryption key storage
- Boot code, firmware storage
- Chip ID and configuration settings

Technology

- Available in 7nm and smaller process nodes
- JEDEC qualified in TSMC N5

Overview

One Time Programmable (OTP) Non-Volatile Memory (NVM) IP solution based on XHF architecture is designed specifically to meet the challenges of advanced FinFET node designs. System-on-chips (SoCs) targeting high-performance compute (HPC), AI, high-end wearables, and edge IoT computing applications require enhanced security, product configurability for end markets, and massive bandwidth. Cost-effective end-product configurability is achieved by embedding field-programmable NVM. Gigabits of embedded SRAM deliver the needed bandwidth, which in turn needs 16 Kbits or more of repair information to be stored on a chip in an NVM. Foundry-provided electrical fuses are easy to hack, are not field programming, and are not area-efficient for storing the required information for SRAM repair.

Synopsys OTP NVM IP is now JEDEC Qualified in TSMC 5nm FF process and is available in flexible configurations ranging from 16 Kbits to 128 Kbits of memory capacity, addressing designers' needs for reliable, secure, field programmable, area and production-cost optimized OTP for next-generation designs. The Synopsys NMM IP solution comprises an OTP memory array with an integrated power supply (IPS) and an OTP controller. The solution supports standard APB interfaces to ease integration into advanced node SoCs. The OTP memory array employs a patented and robust anti-fuse bit-cell designed to operate at low core voltages in advanced FinFET nodes. The bit cell operates on gate oxide breakdown as a programming mechanism and can be manufactured without any additional masks or process steps, making it cost effective, reliable, and scalable. The bitcell is intrinsically secure, making it virtually impossible to distinguish between programmed vs unprogrammed locations upon visual inspection.

Synopsys XHF OTP NVM IP Solution Details

The XHF architecture is designed for robustness and ease of integration into an SoC. It combines the OTP memory array and IPS into a single hard macro and adds wrapper logic to interface with the external world. The solution also includes an OTP controller with standardized APB interfaces delivered as a soft

RTL macro, as represented in Figure 1.

The OTP memory array has a standard data width of 32 bits and includes additional bits in each word to support reliable operation and security at advanced FinFET nodes. Each word in the memory array has repair resources to repair a leaky bit and/or a programming failure. The three-lot silicon qualification in TSMC N5 shows no failing bits under standard JEDEC testing for OTP operating under the specified temperature and voltage conditions, which means all 48 bits, including the repair bits, can potentially be used as data bits. Direct reading of the OTP from the core supply voltage (TSMC N5 OTP only) ensures minimal stress on the OTP during reads, ensuring unlimited reads. The memory array also has word-level lock bits that can be independently set for reads and writes.

The IPS, including a high-voltage charge pump required for programming, is delivered as a hard macro. The solution supports programming one physical bitcell at a time. Before programming, all physical bits within the memory array are unprogrammed. Multiple read modes are supported, and programming depends on the read mode. If using the redundant mode requires two physical bitcells to represent a logical bit, it is necessary to program both physical bitcells of the bit that need to represent a logic 1 and leave both physical bitcells unprogrammed to represent a logic 0.

The wrapper logic includes multiple registers to configure the OTP for reads and writes. The wrapper also includes macro-level read and write locks that grant or deny permission for reads and writes. Additionally, it incorporates an ECC and repair engine. If the extra ECC bits in the OTP memory array are programmed, the ECC and repair logic can repair one random error, one leaky bit and/or one programming failure per word.

The OTP controller interfaces with the OTP through the wrapper logic and provides standard APB interfaces to interact with the world external to the OTP. There is a dedicated and secure APB interface for programming and testing the OTP and another for the read data to be output from the OTP. The OTP controller facilitates reading and writing to the OTP memory array, performs BIST, and performs row replacement/word-level bit-repair as needed. The OTP controller simplifies production test flow.