

DSP Option for ARCV1 Cores

Highlights

- ▶ Separate memory banks for X and Y operands
- ▶ DMA moves data in and out of XY memory
- ▶ Deliver data at register speed
- ▶ Eliminate main memory fetch cycles
- ▶ High performance address generators
- ▶ Address generators operate in several addressing modes
- ▶ Fast pointer accesses
- ▶ 10% of size of DSP coprocessor
- ▶ Single processor solution
- ▶ Can replace separate DSP
- ▶ Up to 32KB/bank (600 family)
- ▶ Up to 64KB/bank (700 family)
- ▶ Support for multiple memory banks
- ▶ Consolidated development environment for both CPU and DSP

Overview

The DesignWare® ARC® XY option gives designers the ability to add the power of a true DSP engine to ARCV1 CPU cores, enabling conventional and signal processing computation within a single unified architecture. The ARC XY option may be applied

Applications

- ▶ Multimedia codecs
 - Audio/Video decoding and encoding
 - Still image manipulation

Dezj@Wysie VBrq|@C X)-t#B (A w)--S4Δ (0)-S0:8 (f)-eS0(μ) #TELEWC \2bsu #L#0 (eu-N2)\WCIDc.i 5\ BDC B.L#3 e (S18 # Δ4e)03 i Tww(i)TELEWC \2bsu #L#0 (eu-N2)\WCIDc.i 58 BDC B.L#3 e (U88\secΔ 4 3 i Tww(e)-e

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