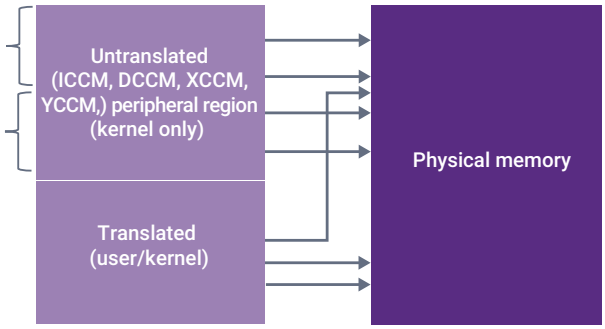
- Lightweight hardware-based memory management unit (MMU) enabling address translation and access permission validation
- Fully associative Instruction and Data µTLBs
- Configurable joint TLB depth of 64, 128 or 256 entries
- Common address space for instruction and data
- Independent rd/wr/execute flags for user/kernel modes per page
- Optimized TLB programming with software managed JTLB and hardware assisted replacement policy
- 32-bit unified instruction/data address space
  - 2GB virtual translated address space, mapping to 4GB physical address space
- Configurable page size: 4 KB, 8 KB, 16 KB
- Per page cache control
- Optional ECC for JTLB RAMs

- AIoT
- Storage
- Wireless
- Networking

The DesignWare® ARC® EM Overlay Management Unit (OMU) option enables address translation and access permission validation with minimal power and area overhead while boosting the ability to run larger and more data intensive operations, such as those increasingly prevalent within AIoT, storage and wireless baseband applications, on an ARC EM processor. This hardware-based Overlay Management Unit provides support for virtual memory addressing with a Translation Lookaside Buffer (TLB) for address translation and protection of 4KB, 8KB or 16KB memory pages. In addition, fixed mappings of untranslated memory are supported, enabling the system to achieve increased performance over a large code base residing in a slow secondary storage memory, with the option to be paged in as needed into faster small on-chip page RAM (PRAM) in an efficient way. This is particularly suited for operating environments in which virtual address aliasing is avoided in software.

In systems that run all code as a single process (single PID), using a large virtual address space with a one-to-one correspondence between the virtual address and a large selected area of secondary storage space (such as flash memory or DRAM), the address-translation facility of the Overlay Management Unit can be used to detect when a section (or one or more pages) of code is resident in the PRAM and provide the physical address to the page in the PRAM.



The EM processor supports virtual memory addressing when the Overlay Management Unit is present. If the Overlay Management