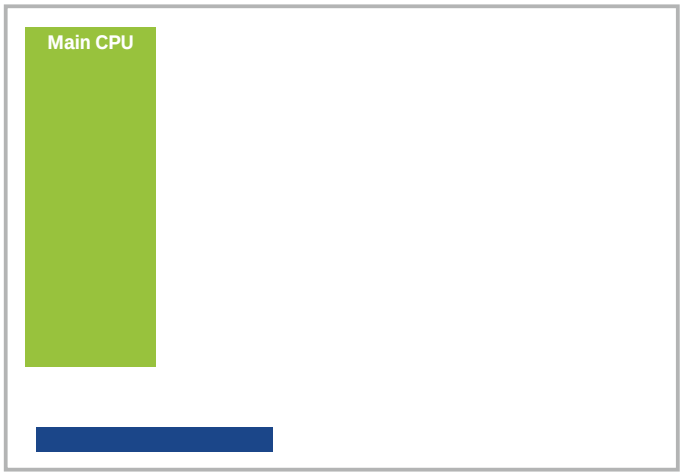
State-of-the-art SoCs incorporate a plethora of analog mixed-signal (AMS) components, such as serializers/de-serializers (SERDES), power conditioners, converters, filters, and high-speed double data rate (DDR) memory (Figure 1). Many of these components require firmware for equalization, calibration, tuning, and configuration. The designs are complex and a challenge


Main CPU

The continual demand for faster computation requires data to be quickly available from memory. This requirement, plus a similar desire for data to be rapidly transferred between systems and their external interfaces, led to the invention of high-speed peripherals, many of which are enabled through complex SERDES components that account for mismatched impedances and other real-world phenomena. Fast memory interfaces operate similarly by embedding the clock signal in the data stream to convert parallel signal paths to/from serial ones. Different applications and operating environments (such as board layout) are accommodated through programming of control registers. For example, for SERDES-based peripherals, the serial output swing can be programmatically increased to reach a longer distance or decreased to reduce power. Similarly, the amount of output de-emphasis can be adjusted based on the link length.

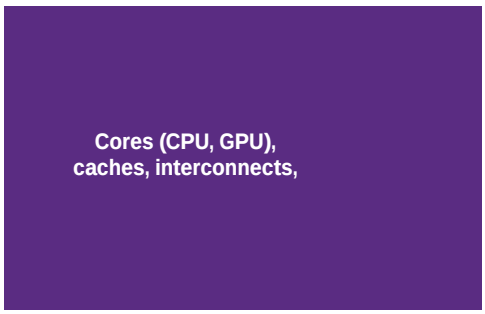
Adapting the hardware to changing environmental conditions is difficult to achieve using fixed parameter values. Instead, the hardware is more agile and extensible if the parameters can be set dynamically, based on real-world phenomena such as PCB impedance. Calibration software performs this role, continuously changing different parameter values and testing their effect on circuit operation to find the optimal settings. Making the SERDES hardware programmable means that it can be tailored to meet the specific needs of a given application [1]. However, hardware configurability must be verified along with proper circuit operation. Therefore, software, such as drivers that control the hardware, must be part of system validation.

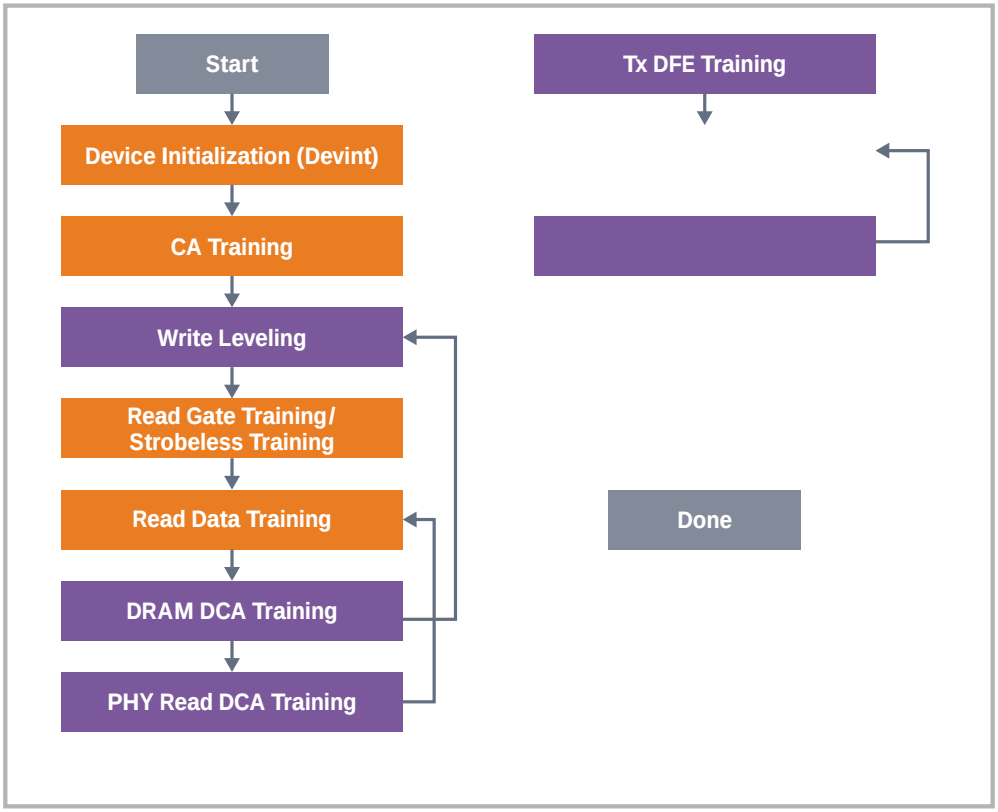
DDR memories share the same need for configurability during system bring-up that cannot be set statically at design time. After power-up and initialization, there are several parameters in a DDR memory that must be calibrated, including [2]:

- Write leveling
- Data strobe (DQS) gating
- Read data eye
- Write data eye

Write leveling adjusts the timing of the write DQS signals relative to the DDR clock. DQS gating determines when the read DQS signal is valid. Read data eye aligns the read DQS signal to the center of the valid read data. Write data eye aligns the write DQS signal to the center of the valid write data.

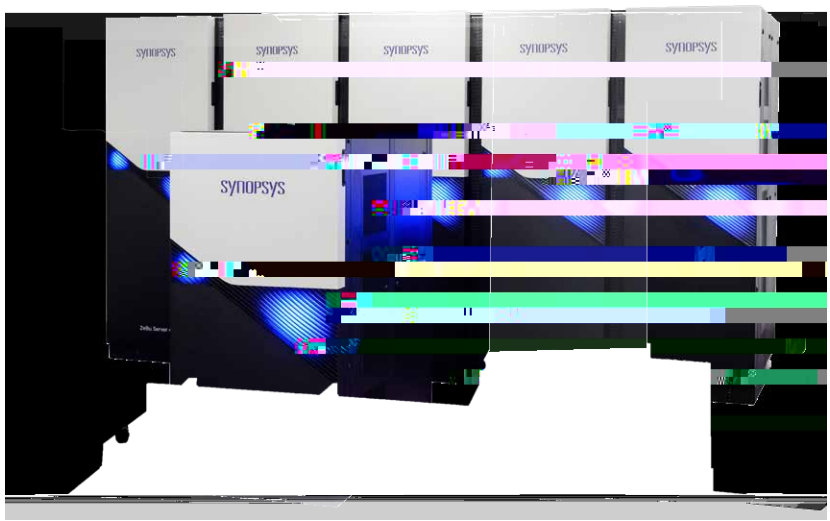
An example of a DDR memory channel is displayed in Figure 3.



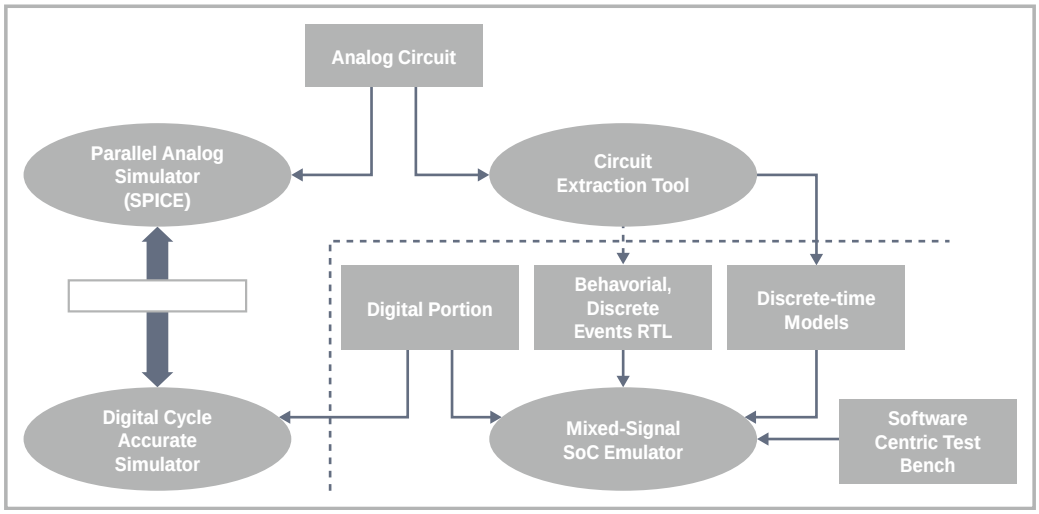

Start
Device Initialization (Devint)
CA Training
Write Leveling
Read Gate Training/
Strobeless Training
Read Data Training
DRAM DCA Training
PHY Read DCA Training
Tx DFE Training
Done

The next challenge is rapid simulation of the DDR RNM model with firmware running on a processor. Digital simulators were enhanced to support RNMs and co-simulate them with digital content. This approach provides about a 10X performance increase over analog simulation but remains too slow for running firmware in conjunction with the models.

Emulation is hardware-assisted simulation. Dedicated hardware, typically based on FPGA technology, provides one or more orders of magnitude performance increase over software simulators such as Synopsys VCS. An example of such a system is the Synopsys ZeBu emulator shown in Figure 5.



Emulation is very good at handling digital circuits. Due to the high speed of digital circuits, they can execute processor cycles fast enough to run software programs up to 10Mhz [6]. This capability enables software and hardware to be verified together pre-silicon. However 1 Tf9 0iysbog136 war(MS RMS,10.1 (eB8softmulamu (ct)9bili(er on a oagni1 Tf co-junctnon-0.1 (ebili(syntax,at)9 (orsfloTmng-pointa


Analog Circuit
Parallel Analog Simulator (SPICE)
Circuit Extraction Tool
Digital Portion
Behavorial, Discrete Events RTL
Discrete-time Models
Digital Cycle Accurate Simulator
Mixed-Signal SoC Emulator
Software Centric Test Bench

Modern SoCs include a mix of analog and digital components. An increasing number of system peripherals require specialized operations, such as calibration and equalization, to optimize their performance in real-world conditions. These operations are performed by software modules, including drivers and firmware. Verification of the complete system mandates validating that the analog, digital, and software interoperate together. This is difficult or impossible to accomplish since each domain—analog, digital, and software—is typically verified independently using different verification tools. The result is that bugs are found post-silicon and often result in costly chip turns that delay time to market (TTM).

Synopsys AMS Emulation technology resolves this problem by enabling full system validation pre-silicon. This unique solution is possible because the Synopsys ZeBu emulator can concurrently simulate analog, digital, and software system elements in hardware at very high performance. This solution is a game-changer for verification of many types of systems featuring components, such as