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Thorsten Gerke
Synopsys GmbH

David Bollati
C&S Group/University of Applied Science Wolfenbüttel

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Thorsten Gerke
Synopsys GmbH

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C&S Group/University of Applied Science Wolfenbüttel

ABSTRACT

Future automotive applications, like high-speed control in power train or drive-by-wire systems, demand large bandwidth, deterministic communication behavior, and fault tolerance. FlexRay, a new standard communication system, is ideally suited to safety applice

cars are already in the range of 40% of the total vehicle development costs. Figure 1 forecasts the increase of vehicle networking protocols used in automotive systems. The complexity of today's vehicle networks has been increasing over the past years and will continue to increase in the future as more content for safety and comfort is integrated into the vehicle. This requires a well-defined and robust in-vehicle network that must guarantee safe and correct data communication while being robust to internal and external influences. This is the challenge of the network engineer responsible for the embedded and physical layer of the network. Unlike the embedded world, the physical layer of in-vehicle networks does not have an ideal logical behavior. There is a significant analog behavior of the physical layer that must be taken into consideration. The dependencies between analog components creates a significant challenge in the design in a system with an infinite number of variants, as no manual computation or any analytical solution exists that describes the complete behavior of the analog network. The following section describes the challenges network engineers face when they deal with the development of the physical layer implementation of FlexRay designs and how this challenge can be addressed using system simulation.

FUNDAMENTALS OF FLEXRAY

FlexRay was created at the end of the 1990's by Automotive OEMs and suppliers. It is intended for applications that need high speed data transfer and time-triggered communication, like closed-loop control systems requiring hard real-time performance. FlexRay allows a variety of topology types while taking into account the physical constraints that are present in a system. Figure 2 shows a possible topology consisting of eight nodes and two active stars. The local timing information of each node is synchronized through the FlexRay protocol. The communication cycle in FlexRay consists of several segments, as shown in Figure 3. All message frames in the static segment have the same length while the lengths of frames in the dynamic segment can be adjusted as needed. Every communication starts with a Transmission Start Sequence (TSS) as shown in Figure 4. The TSS is a continuous low for a period defined for the network cluster and is used to open the gates of active stars and indicate the start of a FlexRay communication. Detailed information about the communication process is given in [1]. Each byte of the payload starts with the Byte Start Sequence (R/T10 -e[u0 0 -1.205t205t2g1 ,sa d to th-8(nc)-8(hr)

- Cascaded active stars
- Hybrid topologies
- Dual channel topologies (including redundant communication channel)

This flexibility provides the network developer the ability to optimize the entire network according to the needs of the application and the vehicle implementation. The selection of hardware components as well as topology type has a significant impact on the signal integrity of the entire system. As shown in Figure 5, bits transmitted by ECU A may arrive in a totally different shape at the receiving ECU F due to the impact of several elements in between each ECU. Items that impact the transmission of signals across the network and are necessary to take into consideration while developing the physical layer implementation include:

- Signal filters (e.g. chokes or ferrites)
- Active stars
- Transceiver
- Transmission line
- ESD protection elements
- Topology type
- Termination

While they allow great flexibility in the design, the developer is faced with the problem that the interaction of all these elements creates a system with analog behavior, and it cannot be determined a priori whether the implementation ensures well-defined signal integrity. Depending on the implementation, the system will exhibit different behavior related to circuit ringing and reflections. In addition, the system developer is also required to ensure sufficient immunity to RF injections.

SIMULATION AS BASIS FOR ROBUST DESIGN

How does a network developer achieve and verify the requirements above and build up a running system that is sufficiently robust to environmental impacts? Development of prototypes takes too much time and is a very inflexible method when evaluating different network options. Simulation is the only choice when it comes to the development of high speed in-vehicle networks like FlexRay or CAN [4]. Simulation allows the creation of network design rules by investigating network limitations through analysis of worst cases and can be used to improve network quality without creating unneeded hardware prototypes. The result is higher quality and significantly reduced development time. Simulation also supports the education process of network designers. Past projects have indicated that network engineers who applied system simulation to the development process know and understand their implementation much better than those who do not, since system simulation allows them to study the electrical behavior to a greater depth than is possible with hardware prototypes alone.

There are several critical aspects of the signal integrity of a FlexRay network that drive requirements for system simulation models for the physical layer implementation. These items are:

- Signal propagation delay
- Asymmetric delay
- Bit deformation due to ringing and reflections
- Truncation of Transmission Start Sequence (transmission idle to busy)
- Frame stretching due to ringing after last frame bit (transition active to idle)

The signal propagation delay is the time lapse between
€

The asymmetric delay describes how much the bit length of the original transmitted bit has changed when it arrives at the receiving ECU. This effect depends on a variety of items, as shown in Figure 7. Some of them have a static dependency, meaning that they are fixed during the communication cycle:

- Mismatches between propagation delays of negative and positive edges
- Hysteresis of common mode chokes
- Parasitic effects (e.g. capacitance coupling due to PCB)

Other effects show a stochastic behavior during the communication cycle:

- Edge Jitter
- Unbalanced behavior above ground

The asymmetric delays are important to be taken into consideration since the higher the asymmetry the smaller

Modeling The FlexRay Node

The model of each FlexRay node, as shown in Figure 10, is a hierarchy containing:

- Transceiver (bus driver)
- Split Termination
- Common mode stabilization circuit
- Common mode choke
- ESD protection (capacitive behavior only)

The transceiver is a model that is delivered by the corresponding IC vendor. For this example, the TJA1080 from NXP Semiconductor (founded by Philips) has been chosen. NXP created a Saber MAST model for this component consistent with the Saber transceiver modeling specification provided by DaimlerChrysler and Volkswagen [6]. Used by the Saber Simulator, MAST is a modeling language for describing Analog/Mixed-Signal components and multi-technology behaviors. The model is not the actual IC transistor level model. Instead, it has been created for the purpose of simulating complete systems, sacrificing some accuracy for speed of simulation. Philips is currently working on adding additional support to the model in order to cover other functional aspects of the transceiver like mode transitions, active star functionality and bus failure detection. The model was validated through measurements against a real system implementation [7].

Transmission Line Model

One of the most important parts of the simulation is the model of the transmission line. The requirements for the transmission line model have been put together by the FlexRay Physical Layer working group who is responsible for defining the FlexRay physical layer specification. Some of the requirements related to the model are:

- Wire length as a model argument to perform wire length variations
- Frequency dependent losses
- Support of both differential and common mode behavior

Saber’s transmission line model addresses all of these requirements. The model equations are defined in the frequency domain to facilitate frequency-dependent effects and then applies a convolution algorithm to get back into the time domain. This method yields significantly better results compared to lumped element approaches which tend to unnecessarily oscillate and are difficult to adapt since the number of cells required for lumped wire models depends on the wire length. The characterization of the Saber model can be done through a field solver computing an RLCG matrix as shown in Figure 11. This approach enables the network engineer the FlexRay EPL application notes [3], the nodes with the boundary violation in the static segment or arbitration issues in the dynamic segment. In the same scenario, the behavior at the low impedance terminated nodes as shown in figure 15 appears to be fine. The behavior at ECU E when ECU C is acting as transmitter should also be considered. Figure 16 shows the corresponding signals at ECU E. The signal shows reflections while the bus is busy during the transition from Low to High and vice versa. The magnitudes of these voltage peaks are 161mV and 192mV respectively. This is still below the input threshold of the transceiver for the nominal case (±225mV) but taking into account that the threshold is ±150mV in worst case due to tolerances of the receiver stage, this may result in multiple switching of the Rxd signal of ECU E. Therefore, it is necessary to damp this signal behavior to ensure a more robust implementation. For the evaluation of the entire system behavior, this analysis must be performed for each single ECU, and the network developer has to validate the complete implementation after introducing any changes. The current implementation would be unacceptable due to the very problematic transition from active to idle. Modifications to the design are needed in order to improve the system behavior from a signal integrity point of view. In order to damp oscillations due to reflections, ferrites are often applied since they damp the reflections in the low impedance center of the passive star. The next implementation contains ferrite cores as passive damping elements (shown in Figure 17) and keeps the same wire length configuration as before.

The same simulation scenario is applied to the design. Figure 18 shows results of the adapted topology. It can be seen that the behavior of the entire topology has been significantly improved by applying additional passive elements. The Rxd signal of ECU B shows much fewer oscillations during the transition from active to idle than before. Still, there is some ringing in the circuit that causes undesired switching of the Rxd signal at ECU B. Two possibilities for dealing with this problem are either to apply ferrite cores with larger signal attenuation or to analyze whether this problem can be handled on the software side. One of the advanced analysis capabilities of Saber is parametric variation. This allows the designer to vary e.g. the inductance value of the ferrites to validate whether a larger ferrite core helps to sufficiently filter the undesired

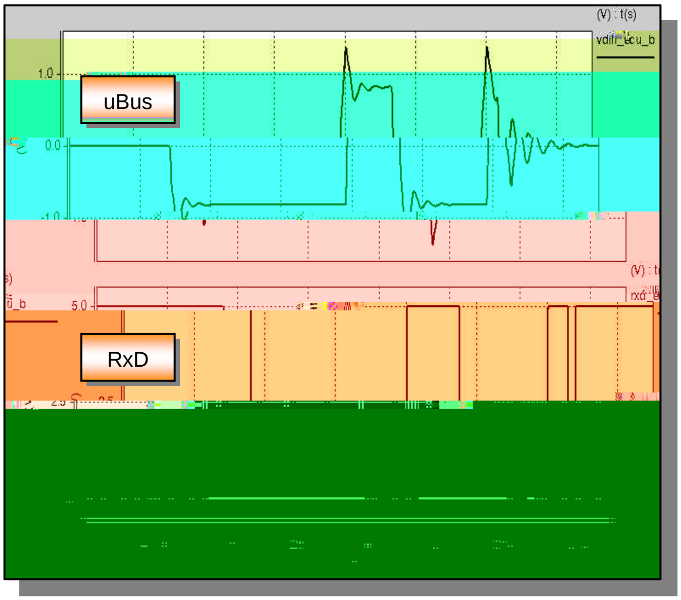

Figure 18: RxD and differential bus signal ECU B (Transmitter ECU D) using ferrites

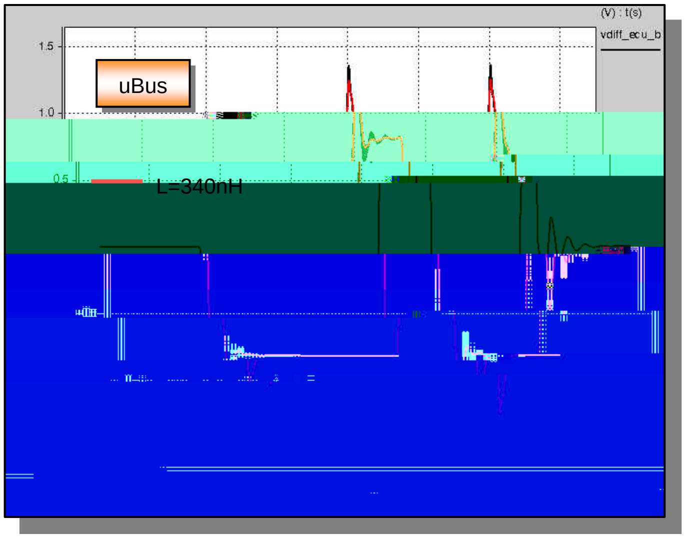

Figure 19: Variation analysis and differential bus signal ECU B (Transmitter ECU D)

ferrite can be applied, while carefully considering the ringing phase during transition from active to idle for the network and frame configuration or looking for other alternatives to optimize the system behavior. An option is for the software engineer to add a certain reserve at the end of the frame to ensure that the ECU is able to detect the network idle state without causing a slot boundary violation. This is the case for some of the other ECUs which have not been shown here. For this scenario, the smaller ferrite is going to be applied. Referring to the previous problem related to ECU E, the ferrites help to remove the undesirable behavior and there is now enough safety margin during the transitions of the logical bus states. Figure 20 shows the results after applying ferrites. It should be noted that this analysis was performed for all nodes in the passive star network.

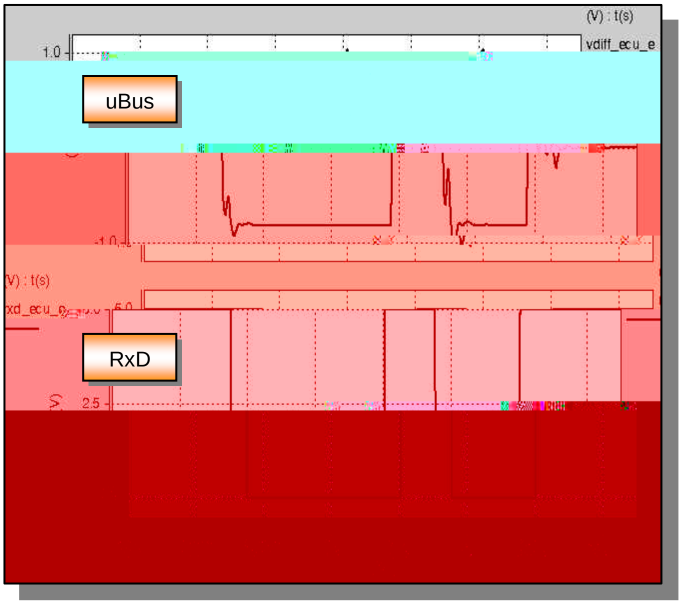

Figure 20: RxD and differential bus signal ECU E (Transmitter ECU C) using ferrites

Simulation can be used to further investigate the performance of the FlexRay network configuration. In order to guarantee that the right bit values are being sampled, it must be ensured that the bit length does not get too corrupted through the transmission across the network. This requires the network developer to validate the asymmetric delays encountered at each individual ECU. In order to analyze this, a single bit needs to be transmitted across the network to check how much corruption is related to the physical layer depending on the signal path. As shown in Figure 21, the asymmetric delay is defined as the difference between actual bit time measured at the transceiver’s digital receive pin and the targeted bit time represented by an ideal bit measured at the transmitter’s TxD pin. The asymmetric delay will be determined for both the High bit and Low bit cases. The FlexRay specification defines limits for the asymmetric delay taking into consideration asymmetric delay due to edge jitter as well as physical layer issues. The maximum allowable asymmetric delay is ±30.75 ns for the complete signal path (e.g. from node A to node B shown in Figure 19). The developer should also take into account some reserve budget for asymmetries due to RF injection or any other uncertainty in the design, as explained in [2]. The physical layer specification does not

4. Development and Verification of In-Vehicle Networks in a Virtual Environment, Thorsten Gerke (Synopsys GmbH), Carsten Schanze (Volkswagen AG), SAE World Congress, Detroit, 2005

5. Physical Layer - Basis of an Automotive Bus using the Example of FlexRay , Prof. Jürgen Minuth (University of Applied Science Esslingen), EESystems Conference, Unterhaching/Munich, 2006

6. Requirements Specification for Transceiver Simulation Models, Carsten Schanze (Volkswagen AG), Harald Bayer, Dietmar Ostowski (DaimlerChrysler AG), 2006

7. Monte Carlo Simulation for Validation of first FlexRay Series Networks, Thomas Suermann (NXP Semiconductors), FlexRay Product Day, Böblingen, 2006

8. TJA1080 Application Notes, Philips Semiconductor

CONTACT

Thorsten Gerke
Application Consultant