## Synopsys Hybrid Prototyping Solution

- Na\_e a,e VI, a à d FPGA- a ed P \_ \_ e
- ▶S,a, ,, ,, , , , , , , , , ea le
- Acieei e i ceeec,i i ,e e e de ⊥ ea - di,e acecii eçi⊥ ad ae
- ▶ ┩aूĻIL SCdeIL , aIIVe ea e Lice
- ► Acceea,e \_,e \_, ebà -
- ▶I e \_ aedeb ııbu
- ► Ea I Â, e a e ARM C, e P ce de, AM A , c, â ac, â d De I Wa e P A, a â e b Id , e

Start Multicore SoC Prototyping Earlier

## Efficient Data Transfer Between Virtual and FPGA Environments

A bid  $\neg$   $\neg$  e e i e b  $\neg$  a ica  $\hat{a}$  d ica  $\hat{a}$   $\neg$ c  $\hat{a}$  e e i a  $\hat{a}$  d  $F^{\bullet}GA$ -ba ed  $\neg$   $\neg$  e.

 F \_ e ica i , eSi
 T i ac, Liba \_ eARM

 AM A \_ c i abe, edaaeci ebe, ei S \_ e C/

 TLM de eec, edb Si
 'Vi, all'e i, a \_ , i

 i da HAPS Seie RPGA-baed \_ , i \_ e .i adduii, ,

 a ea eC++, ac, iba \_ i a icaii

 a i a, e ace (API) i a ai abe daa, ea i

 a icaii
 , e aii be, ei a HAPS Seie \_ e id

 c \_ C++ i i i , .T eSi
 T i ac, Liba

 \_ a aie, ARM AM A \_ c , c , c d AM A 2.0

 AH \*/AP \*, AXI3\*, AXI4\* i d AXI4-Lue\*.

T e ARM AM A a, e c i, c i, ia, ea, i, ac, ie, e, e, V, aller, a , i HAPS FPGA-ba ed  $\neg$ , i, i, i, i, i, e, a, iAPI ide i d, ecere, i d ca bac i, c, i, c i ica, e $\downarrow$ , e ad a ed i, i, e ad a e c i, e, r, e F b c c i ica, e, -, e a e i d a, e, -, c i ica, e $\downarrow$ , e e F.

T  $e_{-}$  i ac, c ed e \_ de- i c i led e a i , e e - i ed de ab , ac i \_ c c e-acc a e FPGA-ba ed a d a e be , e a , e e i c e.

Teae icacili eçil ,, eHA+PS Qi i e a M , i-Re ce (UMR) ) , e ace , i c de a+PCIE e ei ea cad , e , , , a, i i d i i , e ace d a HA+PS Seie , e.

## Naturally Partition With a Hybrid Approach

Childe, ecale  $\neg$ , i, endidac i, ac eSCdeil. Wiehbc  $\downarrow$  a  $\neg$ ecd  $\neg$ a e a i, a FPGA-baed  $\neg$ , e, e den id i, e a i, e  $\neg$  ch a da a ica  $\cdot$  P, e den id i, e a i e  $\neg$ , ch a da a ica  $\cdot$  P, e a, ib, e c a ca act, e  $\neg$ , a, i e b c id ea d i/O acce ch i  $\downarrow$ , ede ee ad ae/  $\neg$  aedee i,  $\neg$ , a ch be acc i ed  $\downarrow$   $\neg$ , i.

, eea eSCdeili, a, aedi Fi e2, eOPU, ee1
d 2 cace e iea ea, edi a ci, e ae d
c dida, e a i, a a ac i ce, ei de a e ea ie
d ice, b, a, i ATL d a e e ce i, , , , , a e e ec, ii. H e e, e, e e i e a c a, e a ic i e d, e adi i, e ace GPS i d WiFi, i d
e e e, , , i freGA, ee, e, a, i d i A e e ce , e aida i .
FRGA-ba ed , a a ad , a e c ce-acc ae e i ce i d de zde, a ei , .

eca e , ead , a e b id , , e de i , ea a e, a , , e di zc , a , c , e FFGA-ba ed , d i, a , e . T i e , i , , i eci , a , de - , e. Si ' b id , , , , ea ed b id , e.



Figure 2: An example of SoC block partitioning between virtual and FPGA-based prototyping environments