Engine c$li)r$tion is t+pic$ll+ performe0)+ $n 3E#, /hile the EC1 co0e is o/ne0)+ the s*pplier of the EC1. -herefore, the 3E# is t+pic$ll+ *n$)le to set *p $n EC1 sim*l$tion)$se0 on the origin$l C co0e of the EC1. 4nste$0, to set *p optimi,$tion on 5C, time cons*ming $n0 error prone reverse engineering is nee0e0 to 0evelop $n 6e.*iv$lent mo0el6 of the EC1 f*nction of interest. -o 0e$l /ith this sit*$tion, /e h$ve implemente0 $ novel metho0 for $*tom$ting the c$li)r$tion of engine p$r$meters. -he metho0 com)ines t/o i0e$s

- sim*l$tion of EC1 progr$m co0e on 5C *sing chip sim*l$tion
- m$them$tic$l optimi,$tion)$se0 on the res*lting exec*t$)le mo0el

-he sim*l$tion re.*ires onl+ the hex, 7%75!8$!l $n0 m$p file, th$t $n 3E# t+pic$ll+ h$s $ccess to,)*t not the so*rce co0e of the EC1 f*nctions of interest.

-his p$per 0escri)es $lso $ pro)lem th$t /e enco*ntere0 /hen co*pling chip sim*l$tion /ith optimi,$tion metho0s th$t re.*ire gr$0ients to g*i0e se$rch for optim$2 prtil 0eriv$tives of engine f*nctions /ith r Äiotn /à $ìe põ0$ res*lt, gr$0ient)$se0 optim

/ith s*)9optim$l sol*tions. -he p$per $lso s(etches i0e$s ho/ to overcome this pro)lem $n0 presents res*lts of n*meric$l experiments.

%im*l$tion h$s gre$t potenti$l to improve the 0evelopment process for EC1s. %im*l$tion helps to move 0evelopment t$s(s to 5C, /here the+ often c$n)e performe0 f$ster, che$per or)etter in some respect :7;. -o exploit these)enefits, the EC1 m*st first)e porte0 to 5C. -his is t+pic$ll+ 0one)$se0 on the C co0e of the EC1, /hich is either h$n0 co0e0, or gener$te0)+ tools s*ch $s 7scet (E-7%), -$rget<in((0%57CE) or Em)e00e0 Co0er (#$th=or(s). &or ex$mple, >-ronic6s virt*$l EC1 tool %ilver :1; provi0es $ fr$me/or(to

- compile given EC1 t$s(s for =in0o/s 5C,
- em*l$te the *n0erl+ing ?-3% $n0 other services (C7@, AC5),
- r*n the res*lting virt*$l EC1 close09loop /ith $ sim*l$te0 vehicle.

-+pic$l $pplic$tions $re :!, ;, /here $ virt*$l EC1 is *se0 to 0evelop the controller for $n $*tom$tic tr$nsmission. &or close09loop sim*l$tion, vehicle mo0els c$n)e importe0 from m$n+ sim*l$tion tools into %ilver, incl*0ing #7-<7B8%im*lin(, D+mol$, %im*l$tionA $n0 #$ple%im, e.g. thro*gh the &#4 form$t for mo0el exch$nge :B;.

Co/ever, sometimes C co0e is not $v$il$)le for implementing $ virt*$l EC1. -here $re t/o m$in so*rces for s*ch $ sit*$tion2

- Protection of intellectual property2 7ll or m$Dor p$rts of the EC1 h$ve)een 0evelope0)+ $ s*pplier $n0 the 3E# intereste0 in)*il0ing $ virt*$l EC1 (e.g. to s*pport c$li)r$tion, $ t$s(t+pic$ll+ performe0)+ $n 3E#) h$s therefore no $ccess to the C co0e.
- Target-specific C code2 C co0e is $v$il$)le)*t the C co0e *ses prgms $n0 other t$rget or compiler specific constr*cts, /hich prevents compil$tion for other t$rgets, s*ch $s the =in0o/s x8 pl$tform.

-o 0e$l /ith s*ch sit*$tions, /e h$ve recentl+ integr$te0 $ chip sim*l$tor into the virt*$l EC1 tool %ilver. -his /$+, $ virt*$l EC1 c$n)e)*il0)$se0 on $ hex file compile0 for the t$rget processor of the EC1. @o $ccess to C co0e is nee0e0 in this c$se. 4nste$0 of compiling C co0e for the =in0o/s x8 pl$tform, the chip sim*l$tor t$(es the)in$r+ compile0 for the t$rget processor $n0 sim*l$tes the exec*tion of the instr*ctions)+ the t$rget processor on =in0o/s 5C. %*ch $ sim*l$tion re.*ires

1. $ hex file th$t cont$ins progr$m co0e $n0 p$r$meters of the sim*l$te0 f*nctions
!. st$rt $00resses of the f*nctions to)e sim*l$te0
". $n 7%75!8$!l file th$t 0efines the conversion r*les for the involve0 inp*ts, o*tp*ts, $n0 ch$r$cteristics, $s /ell $s correspon0ing $00resses

-he st$rt $00resses of f*nctions c$n e. g.)e extr$cte0 from $ m$p file gener$te0 together /ith the hex file. %ilver *ses the $!l file to $*tom$tic$ll+ convert sc$le0 integer v$l*es to ph+sic$l v$l*es $n0 vice vers$ 0*ring sim*l$tion. %*ch $ chip sim*l$tion mo0el c$n $lso)e exporte0 $s %&*nction (mex/"! file) for *se in #7-<7B8%im*lin(. 3n $ st$n0$r0 5C, hex sim*l$tion r*ns /ith $)o*t B0 #45%. 4f onl+ sim*l$ting selecte0 f*nctions of $n EC1, this is f$st eno*gh to r*n $ sim*l$tion m*ch f$ster th$n re$l9time.

-he p$per is str*ct*re0 $s follo/s2 %ection ! 0escri)es ho/ to *se chip sim*l$tion to)*il0 $n0 r*n $ virt*$l EC1 on 5C. 4n section ", /e report ho/ the res*lting EC1 mo0el h$s)een co*ple0 /ith n*meric$l optimi,$tion to $*tom$te engine c$li)r$tion.

s*ch $s $ngle positions re$che0)+ the cr$n(sh$ft. -hree (in0s of t$s(s c$n)e 0isting*ishe0

1. t$s(s th$t gener$te sign$ls, e.g.)+ re$0ing sensors or C7@ mess$ges
!. t$s(s th$t comp*te o*tp*t sign$ls from inp*t sign$ls
". t$s(s th$t *se sign$ls to comm$n0 $ct*$tors or to cre$te C7@ mess$ges

-he t$s(s of c$tegories 1 $n0 " t+pic$ll+ 0epen0 on 0et$ils of the p$rtic*l$r chip (s*ch $s h*n0re0s of registers of on9chip 0evices), $n0 on the EC1 h$r0/$re. 4n contr$st, t$s(s of c$tegor+ ! $re f$irl+ in0epen0ent from s*ch h$r0/$re9specific 0et$ils. -o sim*l$te EC1 co0e, it is therefore convenient to r*n onl+ t$s(s of c$tegor+ !. -he re.*ire0 inp*ts for these t$s(s c$n either)e t$(en from me$s*rement files (open9loop sim*l$tion), or the+ $re comp*te0 online)+ some pl$nt mo0el (close09 loop sim*l$tion),)+p$ssing the t$s(s of c$tegor+ 1. <i(e/ise, the o*tp*ts of c$tegor+ ! t$s(s c$n)e 0irectl+ comp$re0 to me$s*rements (open loop) or fe0 into the pl$nt mo0el (close0 loop),)+p$ssing the c$tegor+ " t$s(s. -he sign$l interf$ce)et/een c$tegories 19! $n0 !9" is t+pic$ll+ /ell 0oc*mente0 $n0 $v$il$)le, e.g. from the C7@ specific$tion (DBC file) of the EC1.

-his mo0elling str$teg+ h$s $ ver+ goo0 cost9)enefit r$tio. 4n or0er to sim*l$te $lso the t$s(s of c$tegories 1 $n0 ", one h$s to mo0el h*n0re0s or peripher$l $n0 chip specific registers, $n0 to)*il0 st$te9m$chine mo0els for lo/9level peripher$ls, s*ch $s C7@ controllers. -echnic$ll+, this is possi)le, e. g. /ith %+stemC :F;,)*t h$r0l+ D*stifie0)+ the $00e0 v$l*e, $t le$st for the $pplic$tion consi0ere0 here.

%ilver !.F *ses $ specific$tion file (simil$r to the 34< file *se0 to config*re 3%EG) to specif+, /hich t$s(s of $ hex file to sim*l$te. %ilver $*tom$tic$ll+ t*rns s*ch $ spec file into $n exec*t$)le %ilver mo0*le (0ll) or %&*nction. 7 t+pic$l spec file loo(s $s follo/s2

```
# specification of sfunction or Silver module
hex_file(m12345.hex, Tri ore!1.3.1"
a2l_file(m12345.a2l"
map_file(m12345.map"      # a T#S$%&' or '&( map file
frame_file(frame.s"       # assem)ler code to emulate *T+S
frame_set(ST-.!S%/-, 10"  # Silver step si0e in ms
frame_set(T-2T!ST#*T, 0xa0000000" # location of frame code

# functions to )e simulated, in order of execution
task_initial(#5 6-!ini"
task_initial(#5 6-!inis7n"
task_triggered(#5 6-!s7n, tri88er!#5 6-!s7n"
task_periodic(#5 6-!20ms, 20, 0"
task_periodic(#5 6-!200ms, 200, 0"

# interface of the 8enerated sfunction or Silver module
a2l_function_inputs(#5 6-"
a2l_function_outputs(#5 6-"
a2l_function_parameters_defined(#5 6-"
```

$ =in0o/s 5C /ith 4ntel iF processor $t !.B EC, $n0 !.9! EB ?7#. 7ver$ge exec*tion times fo*n0 this /$+ $re sho/n in -$)le 1.

		"#
4nfineon tsim	919.1F sec	0.B1
%ilver mo0*le	9."0 sec	B0.80

Ta″le 1: Perfor#ance of chip si#ulation for the BGLWM e$a#ple

-he EC1 consi0ere0 here (#ED17 /ith -C1797) r*ns $t !00 #C, $n0 h$s $ perform$nce of $)o*t "00 #45%. @evertheless, on the EC1, the exec*tion time for the ".F min*tes scen$rio is of co*rse ex$ctl+ ".F min*tes, 0*e to the re$l time constr$int. 3n $ 5C, this f*nction r*ns !0 times f$ster.

$ " % &' (

%ilver c$n $lso t*rn $ spec file $s 0escri)e0 in section !.1 into $ %&*nction, i.e. $ mex/"! file th$t r*ns in %im*lin(. -his is p$rtic*l$rl+ interesting /hen *sing chip sim*l$tion to s*pport $*tom$te0 optimi,$tion of p$r$meters,)ec$*se m$n+ optimi,$tion tools $re implemente0 on top of #7-<7B8%im*lin(. -he gener$te0 %&*nction $ccepts $ll ch$r$cteristics liste0 in the spec file $s %&*nction p$r$meters. -his m$(es it e$s+ to connect the gener$te0 %&*nction /ith $n optimi,$tion proce0*re. &or ex$mple, the %&*nction c$n)e c$lle0 /ith /or(sp$ce vri)les th$t $re then $*tom$tic$ll+ v$rie0)+ the optimi,$tion proce0*re)et/een %&*nction c$lls. -he perform$nce of $ gener$te0 %&*nction is $g$in $)o*t B0 #45%.

!

=e h$ve com)ine0 chip sim*l$tion $s 0escri)e0 $)ove /ith $ proce0*re for n*meric$l optimi,$tion to comp*te optim$l v$l*es for cert$in engine p$r$meters. -hese comp*t$tions re.*ire $n $cc*r$te $n0 f$st mo0el of the engine f*nction of interest. 4n the p$st, /e h$ve *se0 h$n09co0e0 mo0els of EC1 f*nctions, 0evelope0 /ith #7-<7B8%im*lin(. -his h$s)een time cons*ming $n0 error prone. =e h$ve no/ prtill+ repl$ce0 these h$n09co0e0 mo0els /ith %&*nctions gener$te0 $*tom$tic$ll+)+ %ilver from $ given hex file. -he gener$te0 %&*nctions prove0 to r*n $s f$st $s their h$n0 co0e0 co*nterp$rts. -he repl$cement of h$n09co0e0 flo$ting9point mo0els)+ gener$te0 fixe09point %&*nctions r$ises the follo/ing pro)lem2 %ome optimi,$tion proce0*res re.*ire gr$0ient inform$tion to g*i0e the se$rch for optim$l p$r$meter v$l*es2 =hen se$rching for $n th$t minimi,es f( ), the 0eriv$tive df/dx is to)e comp*te0 0*ring optimi,$tion for 0ifferent v$l*es of x. &inite 0ifferences $re often *se0 here2 df/dx is comp*te0 $s (f(x + h) - f(x)) / h for sm$ll h, s$+ h H 10^{9} . 4f f is comp*te0 *sing chip sim*l$tion, x $n0 x+h $re often)oth m$ppe0 to the s$me integer, res*lting in $,ero gr$0ient. 7s $ conse.*ence, the optimi,$tion proce0*re is l$c(ing g*i0$nce, $n0 might ret*rn $ s*)optim$l sol*tion.

-his section presents i0e$s ho/ to overcome this pro)lem $n0 some res*lts of n*meric$l experiments. -here $re $lso so9c$lle0 0eriv$tive9free proce0*res for optimi,$tion. 3)vio*sl+, these $re not $ffecte0)+ the $)ove pro)lem. -his is exploite0 in :8;.

! %)

3ptimi,$tion in engine 0evelopment c$n fre.*entl+)e form*l$te0 $s le$st9s.*$res optimi,$tion. -he o)▯ective is then to minimi,e $ go$l f*nction

$$g(x)=\sum_{i=1}^{m} f_i^2(x) \qquad (1)$$

/here x is $ vector of n re$l v$l*e0 p$r$meters. 7 t+pic$l $pplic$tion is c*rve fitting. -he engine controller cont$ins $ f*nction model(x, t) th$t estim$tes $ ph+sic$l .*$ntit+ th$t the controller c$nnot me$s*re 0irectl+. -his mo0el nee0s to)e c$li)r$te0)+ choosing p$r$meters x s*ch th$t $ me$s*re0 series of m 0$t$ points is pre0icte0)+ the mo0el $s goo0 $s possi)le, i.e. the s.*$re0 s*m of the m re$l9v$l*e0 resi0*$ls

$$f_i(x)=\mathrm{model}(x,t_i)-\mathrm{measurement}(t_i) \qquad (!)$$

gets minimi,e0. 4n t+pic$l $pplic$tions, there $re h*n0re0s of 0$t$ points $n0 p$r$meters.

7lgorithms t+pic$ll+ *se0 for le$st9s.*$res optimi,$tion $pproxim$te for 0ifferent choices of x the '$co)i$n

$$J_{i,j}(x)=\lim_{h\to 0}\frac{f_i(s(x,j,h))-f_i(x)}{h} \qquad (")$$

$$s_k(x,j,h)=\mathrm{if}\ (j=k)\ \mathrm{then}\ (x_k+h)\ \mathrm{else}\ x_k$$

to 0etermine $t $ given point x in p$r$meter sp$ce the 0irection of steepest 0escent of g(x). E$ch element of the $)ove '$co)i m$trix is t+pic$ll+ $pproxim$te0)+ $ finite 0ifference

$$D_{i,j}(x)=\frac{f_i(s(x,j,h))-f_i(x)}{h} \qquad (B)$$

/ith s*fficientl+ sm$ll h, s$+ h H 10^{9} .

! *

Engine controllers $re fre.*entl+ implemente0 *sing fixe09point co0e, i.e. $ll comp*t$tions $re performe0 *sing integers, not flo$ting point n*m)ers. 7s $ conse.*ence, /hen implementing the go$l f*nction g (or ▯*st the resi0*$ls f) *sing

4n gener$l, /hen optimi,ing go$l f*nctions implemente0 *sing chip sim*l$tion /ith

v¾cR[illegible]

r*gge0 l$n0sc$pe seen in &ig. !d $n0 h. -he const$nt f$ctor k is intro0*ce0 to compens$te this. &or ex$mple, choosing k H 10 verges the 0eriv$tives $cross 10 gri0 points, /hich re0*ces the noise gener$te0)+ integer ro*n0ing.

&or given x, e$ch element of the m$trix H(x) c$n)e comp*te0)+ se$rching for the lo/er (min

3ne interesting point is cross9comp$rison of fo*n0 sol*tions2 -he h$n0 co0e0 %im*lin(mo0el gener$te0 $ sol*tion xOptSimulink /ith

gSimulink(xOptSimulink) H 0.01B8

/hile optimis$tion /ith chip sim*l$tion gener$te0 $ slightl+ 0ifferent sol*tion xOpt hipsim /ith

g hipsim(xOpt hipsim) H 0.01B9

Cross9comp$rison sho/s th$t)oth go$l f*nctions 0efine slightl+ 0ifferent optim$2

gSimulink(xOpt hipsim) H 0.0!00

g hipsim(xOptSimulink) H 0.0!17

-he go$l f*nction g hipsim is ho/ever $)it $cc*r$te mo0el of the comp*t$tion of the re$l engine controller, /hile gSimulink is $ h$n09co0e0 mo0el /ith $ cert$in mo0eling error. =e therefore)elieve th$t on the re$l engine controller, the sol*tion fo*n0)+ chip sim*l$tion performs effectivel+)etter (0.01B9) th$n the one fo*n0)+ the h$n09 co0e0 %im*lin(mo0el (0.0!17).

$

7s 0emonstr$te0 $)ove, $n EC1 hex file compile0 for some t$rget processor c$n)e exec*te0)+ the virt*$l EC1 tool %ilver on =in0o/s 5C, either open9loop 0riven)+ me$s*rements or in close09loop /ith $ vehicle mo0el. Depen0ing on the $pplic$tion, selecte0 EC1 f*nctions $re sim*l$te0, or ne$rl+ the entire EC1. 7s sho/n in section ", s*ch chip sim*l$tions c$n)e co*ple0 /ith optimis$tion proce0*res.

-his (in0 of sim*l$tion opens ne/ possi)ilities to move 0evelopment t$s(s from ro$0, test rig or Ci< to 5Cs, /here the+ c$n)e processe0 f$ster, che$per or)etter in some respect, /itho*t re.*iring $ccess to the *n0erl+ing C co0e. D$imler c*rrentl+ *ses this innov$tive sim*l$tion $ppro$ch to s*pport controls 0evelopment for g$soline $n0 0iesel engines, see $lso :8;. 3ther $pplic$tions, s*ch $s online c$li)r$tion on 5C vi$ AC5 seem to)e 0o$)le $s /ell.

-

:1; 7. '*ngh$nns, ?. %er/$+, -. <ie)e,eit, #. Bonin2 B*il0ing Lirt*$l EC1s >*ic(l+ $n0 Economic$ll+, 7-M ele(troni(0"8!01!, '*ni !01!. %ee ///.7-Monline.0e or http288.tronic.0e80oc87-MeN!01!Nen.p0f

:!; C. BrOc(m$nn, '. %tren(ert, 1. Geller, B. =iesner, 7. '*ngh$nns2 #o0el9)$se0 Development of $ D*$l9Cl*tch -r$nsmission *sing ?$pi0 5rotot+ping $n0 %i<. 4ntern$tion$l LD4 Congress -r$nsmissions in Lehicles !009, &rie0richsh$fen, Eerm$n+, "0.0 .901907.!009. http288.tronic.0e80oc8DC-N!009.p0f

:"; G. ?Pp(e (e0.)2 Design of Experiments (DoE) in Engine Development 9 4nnov$tive Development #etho0s for Lehicle Engines. Expert Lerl$g, !011.

:B; -. Bloch/it,, #. 3tter et. $l.2 &*nction$l #oc(*p 4nterf$ce !.02 -he %t$n0$r0 for -ool in0epen0ent Exch$nge of %im*l$tion #o0els. 9th 4ntern$tion$l #o0elic$ Conference, #*nich, !01!.

:F; %+stemC, <$ng*$ge for %+stem9<evel #o0eling, Design $n0 Lerific$tion, see ///.s+stemc.org

: ; #. -tr, ?. %ch$ich, -. Breitinger2 7*tom$te0 test of the 7#E %pee0shift DC-control soft/$re. 9th 4ntern$tion$l C-4 %+mposi*m 4nnov$tive 7*tomotive -r$ns9missions, Berlin, !010. http288.tronic.0e80oc8-est=e$verNC-4N!010Np$per.p0f