# VC SpyGlass RDC

## Comprehensive, scalable, low noise reset verification

## Overview

Clock domain crossings (CDCs) are a well-known source of metastability, but they are not the only source. Asynchronous reset crossings within the same clock domain can also cause metastability. The use of asynchronous resets is becoming more prevalent because of the broader use of multi-phase power-up boot sequences and increasing software asynchronous resets. Therefore, designs are now more prone to expensive Reset Domain Crossing (RDC) issues, which can add significant time and cost to design and debug cycles and may even escape in silicon resulting in expensive respins. Like CDC verification, RDC verification has become equally essential signoff criteria to ensure that the designs work per the specifications.

## Introduction

Three critical measures determine the practical value addition of static RDC verification tools:

1. Time taken to sign off the RTL
2. Completeness and comprehensiveness of RDC verification
3. Flexibility in achieving closure for RDC signoff

VC SpyGlass™ RDC is built on a highly scalable VC SpyGlass RTL Signoff platform that provides a comprehensive methodology with scalable capacity for quality signoff with high debug productivity to address all three criteria.

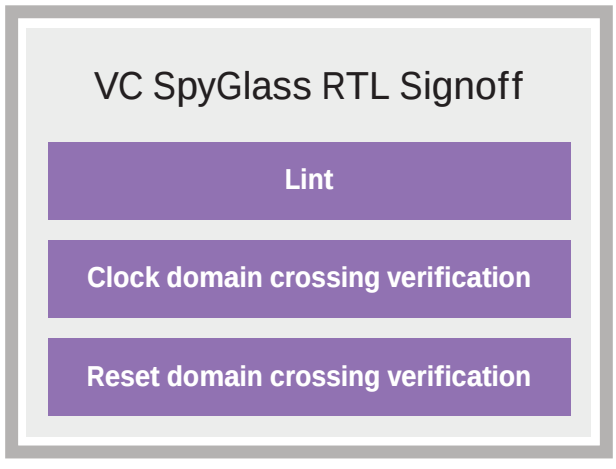
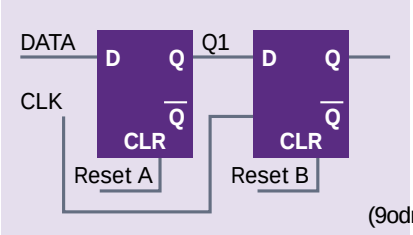
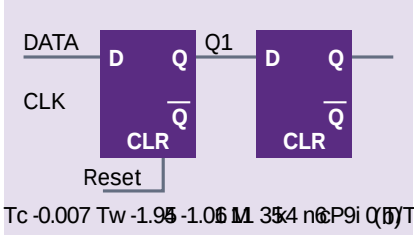



Figure 1: VC SpyGlass RTL Signoff solution

## RDC Bug Examples

RDC bugs are caused due to asynchronous reset assertions on the launched sequential flop without honoring receiving sequential clock's arrival, resulting in timing violations causing metastability issues.



## Separating True from False Violations

To accurately isolate reset domain crossing issues, it is necessary to recognize industry-standard design techniques to identify safe RDC crossings. These techniques include:

- Disabling clock, data or enable of the destination flop
- Taking user-defined reset sequencing into account
- Recognizing synchronization techniques (e.g., Qualifiers, isolations, static signals, etc.)

The result of this accurate analysis is a significant reduction in noise. This effort includes time spent upfront on the correct setup, enabling accurate analysis with minimal noise. VC SpyGlass RDC provides a step-by-step approach to develop an efficient setup for comprehensive RDC verification.

## Power-Aware RDC Verification

Power domains and resets go together and usually each power domain has its own resets. These resets' assertion and de-assertion sequencing are supposed to be aligned with respective power domain transitions.

Since UPFs aren't considered for RDC Verification at the RTL level, all low power signals are unconnected, resulting in the following critical gaps in verification.

1. Unanalysed (hidden) paths can manifest as asynchronous reset domain crossings in silicon
2. False violations for RDC paths which could be blocked due to UPF isolations