ESP

Custom Design Formal Equivalence Checking Based on Symbolic Simulation

High-quality equivalence checking for full-custom designs

Overview

ESP is an equivalence checker for full custom designs. It enables efficient comparison of a Verilog reference design against other Verilog models or a transistor-level SPICE netlist.

ESP provides fast and extensive coverage, enabling users to quickly find bugs and have the confidence that the Verilog reference design is functionally identical to other Verilog models or its transistor-level implementation.

ESP improves overall verification productivity by simplifying the testing process. It directly verifies the SPICE netlist, eliminating the need to manually extract the transistor network into a gate-level representation.

Verification Scope

ESP verifies that two different design representations are functionally equivalent. These designs may be described as Verilog behavioral models, RTL, UDP's, gates, transistors, or SPICE netlist views (Figure 1).

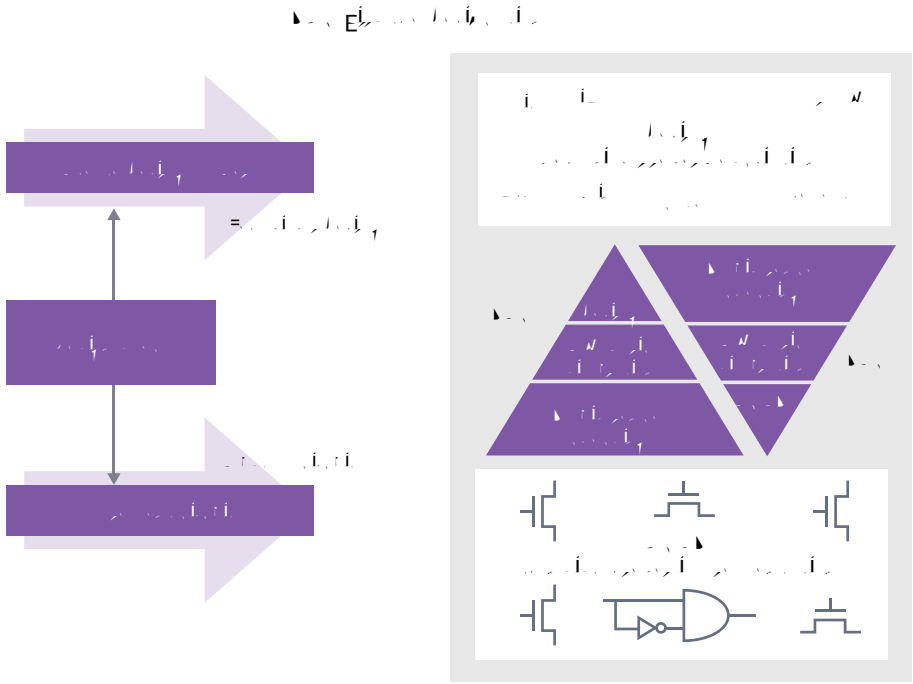


Figure 1: Bridging the verification gap between Verilog and SPICE

Benefits

Higher Quality

ESP provides fast and complete coverage, enabling you to quickly find bugs and have the confidence that the reference model is functionally identical to the transistor model.

Increased Productivity With ESP, you no longer have to derive directed and random tests or have a long delay in releasing models while you complete your verification suite.

Easy to Use

ESP directly verifies the SPICE netlist, eliminating the need to manually extract the transistor network into a gate-level representation.

Memories are Changing

Over 50 percent of the total silicon real estate in today's SoC is consumed by memories. And as designs move toward sub-nanometer process technology, functionalities such as redundancy, ECC, BIST, pipelining, etc. are being added to these designs, resulting in significantly higher functional complexity.

With few standards and many degrees of freedom, functional verification of embedded memories has become a critical need in the SoC design verification process. A key requirement of a successful design is that the behavioral reference model used for SoC full chip simulation is functionally identical to the transistor-level netlist that represents the actual implementation.

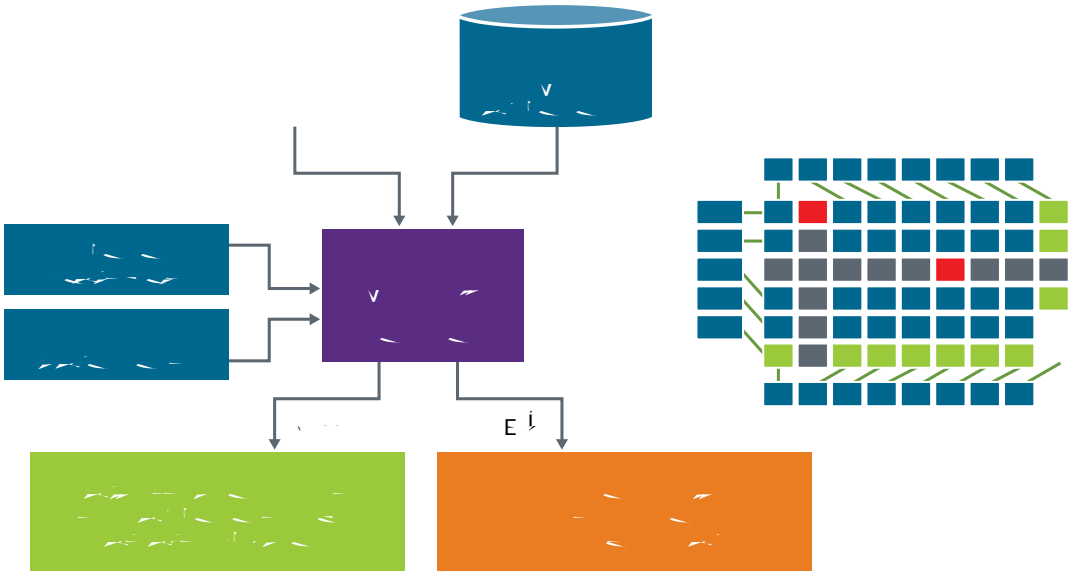
ESP simultaneously simulates two different design representations using symbolic inputs while observing the outputs of each representation to assure equivalent responses. Instead of applying all possible combinations of binary states, ESP applies a symbol that represents all possible input states. This results in coverage of 2N possible states with only N number of symbols (Figure 3A).

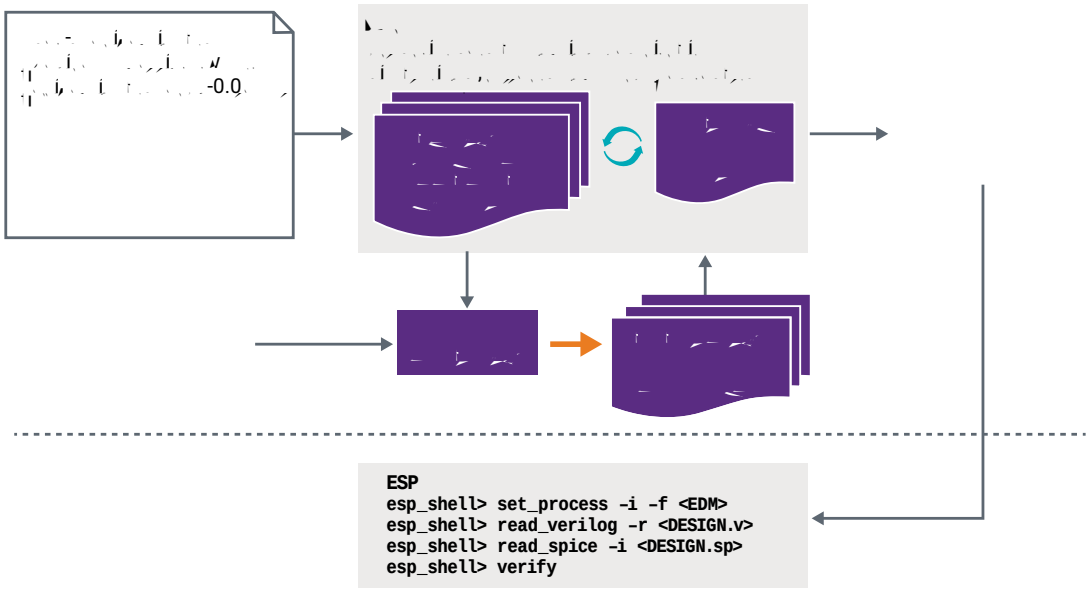
ESP is capable of applying formal verification to the circuit-level designs, delivering an easy-to-use verification solution that is circuit-aware.

Unlike other methods that require modeling of transistor-level designs to cell-based gate equivalent netlists, ESP directly verifies the functional equivalence of the SPICE-level netlist against a behavioral or RTL representation of the design. ESP greatly simplifies the inclusion of transistor parasitic effects in the functional model by automatically calculating the RC value based on transistor length, width, and process technology (Figure 3B).

Redundancy Verification Flow

ESP uses formal techniques to quickly verify that the redundancy logic added to the memory array to replace defective cells and improve yields is performing correctly (Figure 5).





```
ESP
esp_shell> set_process -i -f <EDM>
esp_shell> read_verilog -r <DESIGN.v>
esp_shell> read_spice -i <DESIGN.sp>
esp_shell> verify
```