Accelerate formal

Overview

SoC design complexity demands fast and comprehensive verification methods to accelerate verification and debug, as well as shorten overall schedule and improve predictability. Synopsys VC Formal™ has the capacity, speed and flexibility to verify some of the most complex SoC designs and includes comprehensive analysis and debug techniques to quickly identify root causes leveraging Verdi® debug platform. The VC Formal solution consistently delivers highest performance and capacity, with more design bugs found, more proofs on larger designs and achieves faster coverage closure through the native integration with VCS® functional verification solution. For customers with limited formal verification experience, extending their verification flow to include formal can be a big undertaking.

About Verification CoStart for VC Formal

Verification CoStart enables customers to accelerate adoption of new technologies and increases productivity in their verification environments.

Verification CoStart for Formal is a 10-day service where Synopsys engages with the customer's verification team to understand the existing verification methodology and how formal verification can be added to the customer's overall verification flow. Synopsys will also train up to 5-customer engineers on how-to run the tool, as well as debugging and interpreting the results.


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