SYNOPSYS®

Semiconductors have always been challenging to develop, with many waves of innovation in electronic design automation (EDA) tools and fabrication technologies barely keeping ahead of ever-growing design size and sophistication. Once again, the industry has reached a tipping point. The combination of increasing chip and system complexity, coupled with higher expectations for product performance and longevity, has defined new boundary limitations in designing, manufacturing and deploying semiconductors. Incremental improvements to traditional methods will not be enough to move forward; a new approach is required.

Silicon Lifecycle Management (SLM) is an emerging paradigm within the industry that will make product development and deployment more deterministic. SLM consists of two primary steps:

- Deploying monitors and structures embedded within silicon designs to gain insight on how devices are made and how they then perform in-field
- Gathering and analyzing data at every opportunity throughout the lifecycle of silicon devices to provide powerful analytics that enable in-design, in-test and in-field observations and device improvements to be made

SLM enables the semiconductor design community to exploit a “monitor, analyze and optimize” philosophy. The key benefits are improvements in quality, performance and reliability of silicon systems, enabling predictive maintenance and failure prediction. These lifecycle insights provide significant capability and performance benefits to forward-thinking users, including those in hyperscaling, consumer and automotive applications.

Synopsys is developing new and insightful SLM monitoring and analytics technologies, under a single platform, that resonate with customer and partner ecosystems. This is one of the most exciting growth sectors of the semiconductor industry and Synopsys has emerged as a significant contributor in this space with its Silicon Lifecycle Management Family.

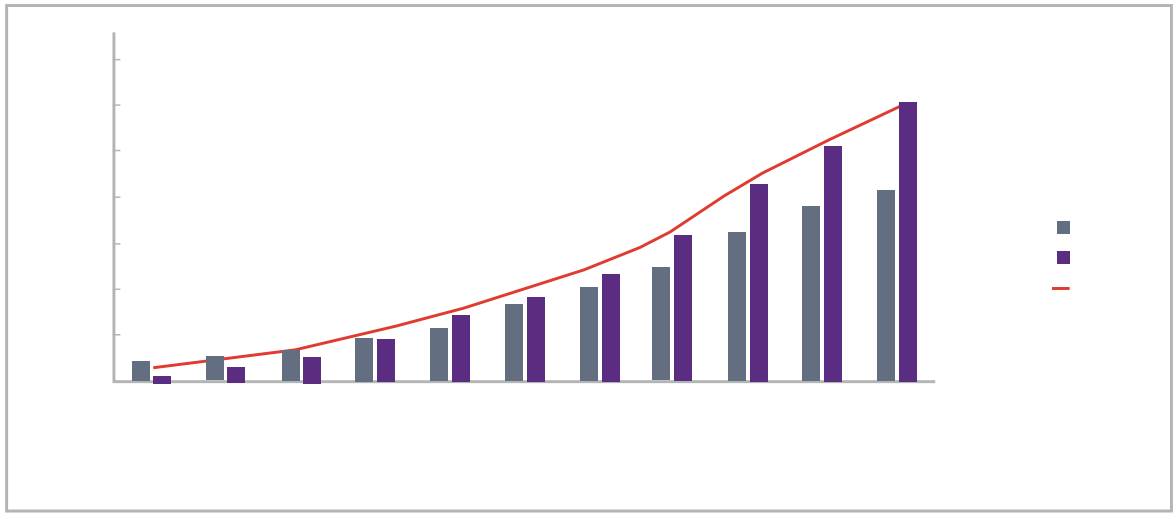
The semiconductor industry is facing new challenges posed by the accelerated scaling of device and system complexity. For each new technology node, transistor densities continue to increase. This provides a great opportunity for adding technology capabilities, but it also great challenges. With increasing transistor density comes more significant variability in the manufacturing process. This broadens the design envelope unless process variability across the die can be measured using monitoring structures.

Increased design density also produces greater current density and, therefore, power density. This presents challenges from diminished advanced node voltage supply levels varying due to dynamic workload activities. The heat dissipated throughout the die due to increased transistor densities is also a challenge, creating hotspots that need to be managed to tame the power conditions and improve the chip's reliability. Other forms of increasing complexity include:

- Chip complexity—placement and routing complexity
- System complexity—die stacked in multi-chip module (MCM) or 2.5D/3D arrangements
- Hardware and software design complexity and interactions—the way the SoC design reacts to stimulus, executes instructions and transacts data is not entirely deterministic through the device's lifetime as firmware and software are upgraded

Greater density and complexity increase the likelihood of physical failure. This, combined with expectations for zero faults in manufacturing and increased longevity in-field, presents additional challenges. Circuit testing must extend beyond the manufacture, bring-up and production test phases to normal operation phases in mission mode in-field. Continuous testing throughout the product's lifecycle is required.

Better and more efficient designs are essential. Figure 2 represents the silicon and software design costs for an advanced performance multicore system-on-chip (SoC) silicon solution. Not every design will reach these cost levels. If the design is a first-time effort, is from one of the first companies to design at a new process node and maximizes all the design parameters (highest possible gate count, fastest speed and largest die area), costs like those shown in the graph can be incurred. Designs with device parameters that are not pushed to the limit may incur lower design costs.

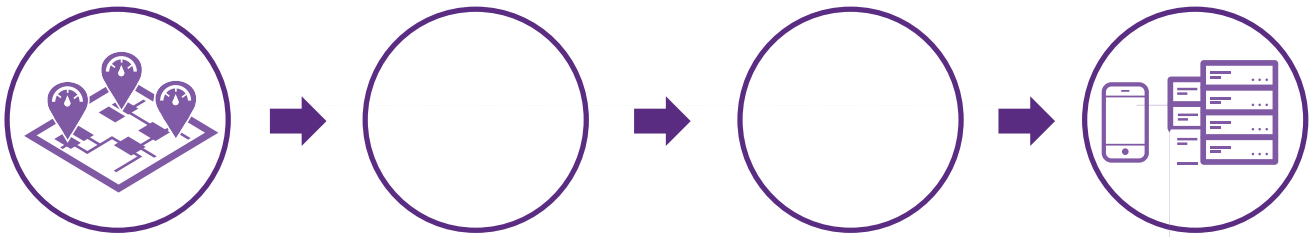


Along with the rising costs associated with each stage of a chip's lifecycle, there are growing amounts of data generated. These can include design data, manufacturing parametric data, test data and in-field data. Data coherency across each of these stages, different users and multiple vendors is an emerging area for the industry. Work in this field may lead to alliances and standards being defined for data capture, formatting, contextualization, consolidation, compression, telemetry, storage and security. These needs, along with the lifecycle analytics that leverage the data, drive the important emerging SLM domain.

Increasing system complexity, compounded with the high performance and reliability expectations of data center, automotive and consumer applications, places high demands on chip developers. In response, the semiconductor industry is required to introspectively examine each process step in the creation and deployment of silicon devices. Such examination will deliver excellent value with higher degrees of data visibility and analytics that lead to optimization actions:

- In-silicon visibility: By embedding monitors, instruments or agents into the design, it is possible to act on conditions of how a device has been made and how it responds to stimuli. There is a strong desire for measurement data that is increasingly more accurate, more distributed and more responsive. As well as the application of embedded structures to measure parametric silicon information, new monitor types are being developed to uncover further information, becoming additional sources for the analysis of static and dynamic data.
- In-test visibility: This includes the application of analytics during test phases to increase the visibility of failing devices and change what is acceptable as a known-good-die, providing comprehensive screening of silicon and expanding the criteria for what is accepted.
- In-field visibility: Deployment of silicon into systems in the field, large sample sets, analytics across entire product ranges or fleets and visibility of longer-term trends are all highly desirable.
- Data accessibility: Users want insightful and meaningful data that has been compressed and contextualized, with web-based graphical user interfaces (GUIs) showing this data appropriately across an organization, from engineers to executives. This ensures that users do not “drown” in raw, voluminous data.

SLM provides all these aspects of data visibility and performs the required analysis on this data. Thus, lifecycle management for semiconductor-based systems is emerging as one of the key areas of investment for the chip industry. Its concepts must be ingrained within the language of design, development, manufacture, production test and quality teams. Successful silicon lifecycle management integrated systems must be built on a unified database solution, capturing and storing pertinent information from each lifecycle stage, as shown in Figure 3. An SLM vendor must provide both native and third-party database solutions depending upon the user’s attitude toward data sensitivity.



- Embedded edge analytics solutions within devices operational in the field
- An ecosystem to enable data telemetry, manipulation, storage, security and analysis across monitors

The SLM system must also be flexible, able to grow and scale over time. It must allow easy adoption of new structures and monitors. It must monitor various aspects of silicon parameters, including those that change over time, such as aging and degradation. The system should accommodate novel “instruments” or “agents” developed by the SLM vendor or third-party partners.

By improving lifecycle visibility, enriched analytics and reporting, SLM enables the semiconductor design community to explore enhanced versions of established control mechanisms. This optimizes device operation for either power or data throughput performance, under the "monitor, analyze and optimize" philosophy mentioned earlier. Key benefits include improvements in the 9xplor. Key benefits includefcn(o i2hy mentione6 638258TLng lif72 (ecy)6.5 (pn .2 4 (e (Tno muchieimiz)5.2 (v)6.loped b)5.77eo e thr)373 (venty)5n

SLM is an increasingly important element of the production, manufacturing and deployment flow for SoCs and other advanced semiconductors. Synopsys has emerged as a key player in SLM with its Silicon Lifecycle Management (SLM) Family, a solution that meets all the requirements and provides all the benefits discussed thus far, including a Unified Database. In addition, Synopsys Silicon Lifecycle Management Family has unique capabilities that position Synopsys as an industry thought leader. Figure 5 shows the key components of this end-to-end solution. These include:

- Embedded monitoring IP, including PVT and path margin
- Digital Design Plat 0fse include:

whether slow, typical or fast silicon speeds dominate) can be formed. This data can be used to tune and calibrate models used in simulation. Thus, the design process is tightened and made less pessimistic, creating an opportunity for silicon area (through better-tuned logic synthesis) and power reduction.

By inserting DFT test structures for scan and built-in self-test (BIST) as a part of the design flow, significant value is provided during chip production to screen for “good” die (as measured by functionality, performance and reliability). Yield Explorer provides design-centric analysis and reporting for DFT and failure analysis for production when ramping to volume. SiliconDash provides production-centric analysis and control to improve quality and productivity, handles large data sets and provides reports via an efficient online user interface. Both Yield Explorer and SiliconDash connect to the SLM Unified Database, offering a coordinated data

SLM is a powerful and flexible concept, and Synopsys SLM leverages this flexibility for application in many different scenarios or use cases. One such use case is Design Links, in which parametric and critical path margin information from silicon manufacturing is fed back into the design flow via Digital Design Family. This silicon-to-design calibration provides several valuable benefits:

- Reduced design margin, reducing simulation over-pessimism
- Optimization of design libraries
- Optimization of ramp to volume by discovering precisely the cells contributing to systematic device failure
- In-field silicon failure debug, assisted by comparing failing transition delay paths within silicon against design tool timing reports