Project Overview

High-speed functional interfaces such as PCIe and USB can perform double duty as high-speed test access interfaces addressing multiple design challenges. Synopsys has collaborated closely with Amazon Web Services (AWS) over the last few years to create and implement a unique solution that leverages an existing functional protocol-based high speed interface for testing and monitoring which has provided a consistent portable method to test silicon throughout its lifecycle.

Challenges

Advanced node and larger chip designs experience numerous challenges in order to achieve reliable silicon operation over their entire lifecycle. Modern SoC's are implemented in many mission-critical applications which require a very low defective-parts-per-million (DPPM) metric. There are two ways to guarantee low DPPM - continuous testing and monitoring of semiconductor devices throughout their lifecycle and increased test coverage. At the same time there is pressure to reduce the number of pins on the SoC, making it difficult to meet test time and cost goals.

Traditional pins used for scan testing operate in the frequency range of 50Mhz—200Mhz. Until a few generations ago, such

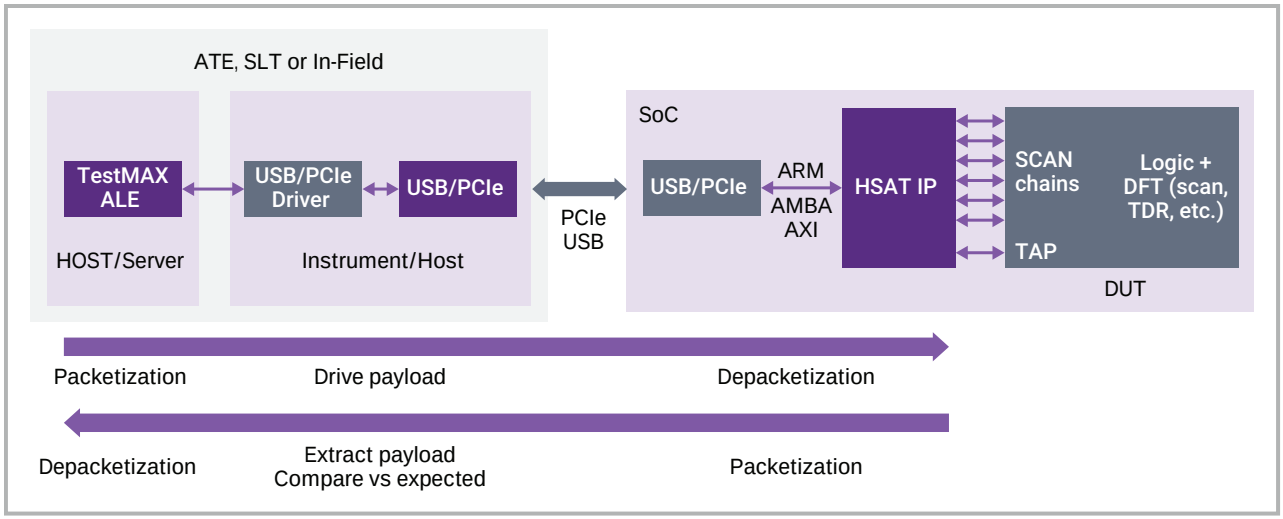

Figure 1: Synopsys SLM HSAT IP solution

Another capability of Synopsys SLM HSAT IP is its ability to leverage the same manufacturing test patterns, functional interfaces, and infrastructure to support System-Level Test (SLT) and In-System Test (IST) without needing access to test pins. The Synopsys SLM HSAT IP solution addresses the bandwidth limitation of GPIO-based interfaces and naturally scales to take advantage of advances in bandwidth of PCIe and USB technology.

Key Benefits of High-Speed Functional Serial Interfaces for Test

- Easily repeat manufacturing tests in-system and in-field
- Reduce test time by eliminating the constraint of GPIO test pin data rate
- Re-use functional HSIO ports (PCIe and USB) for test and monitor data
- Avoid the need for large numbers of GPIO test pins
- Bandwidth scales with each new generation of PCIe/USB

Architecture for AWS ML Server