

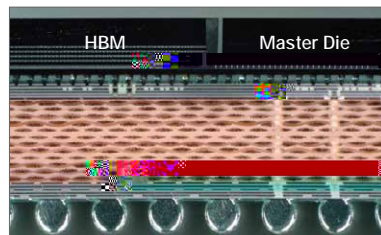
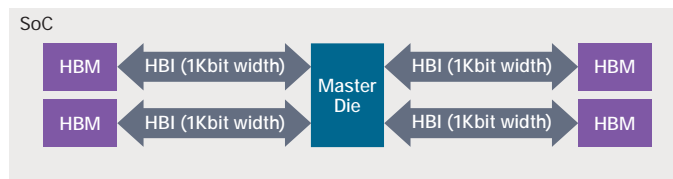
a cross-functional team to satisfy the design or test (D) requirements on a challenging on-chip system (SoC) project in a shorter time to market and four High Bandwidth Memory (HBM) modules. We completed all demands successfully shipped the product on schedule, at the target data rate, and without any impact on logic die size.

~Shinichiro Ikeda, Senior Principal Engineer, Socionext Inc.



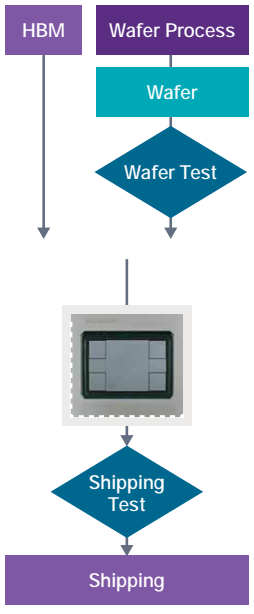
## Challenges

## Project Overview



Silicon Interposer

Package Substrate (Organic) ISIP BGA Balls



	Test Flow	Test Item	WT	FT	DA
(a)	Master Die Test	Master Die Test (including other IPs)			-
		Master die logic scan test (including PHY IP)			-
SLM SHS IP	(b)	HBM PHY IP Test			-
		At speed loop back test			-
	(c)	HBI Connection Test and Repair	-		-
SLM SMS ext-RAM IP	(d)	HBM DRAM Test	-		-
		HBM DA Test	-	-	

