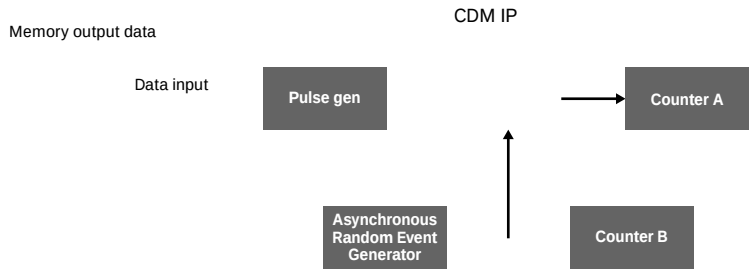

CDM IP
Memory output data
Data input
Pulse gen
Counter A
Asynchronous Random Event Generator
Counter B

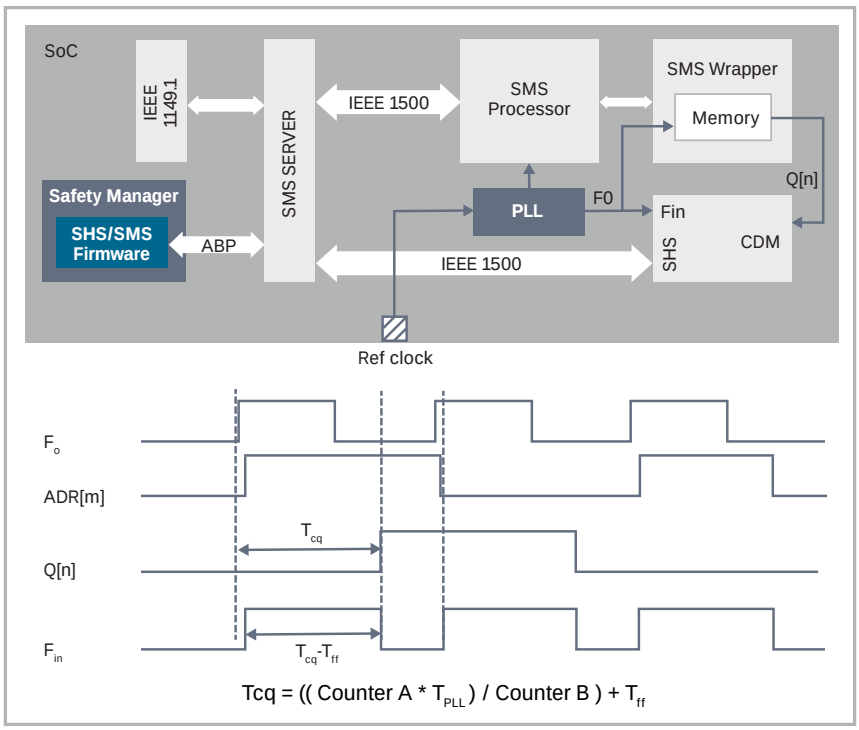
Key Features

- No high-speed high accuracy reference clock required
- Small footprint
- Available as soft IP with flexibility to customize

Key Benefits

- Clock duty cycle quality check
- Memory access time tracking with BIST
- Digital delay line test characterization
- Optimize silicon performance for safety critical applications

Complete solution in SHS/SMS environment for Memory Read Time



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