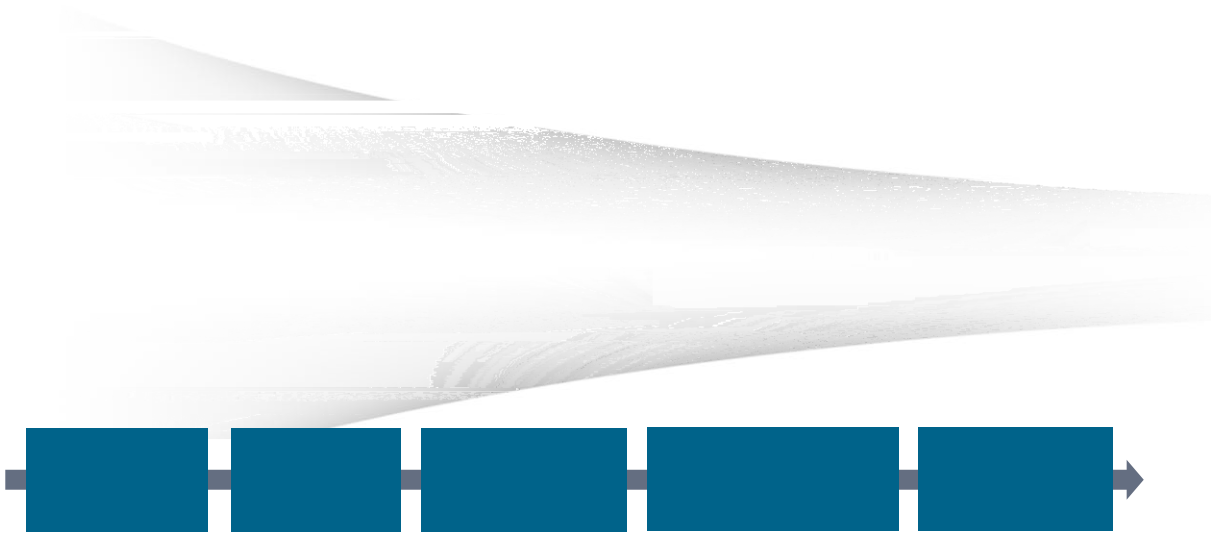
Introduction

It takes a great deal of energy to power the modern world, and demand grows every day. This is especially true for electronics, where ever increasing automation and more intelligent devices

Every additional watt consumed must come from somewhere, and the cost to keep up with this demand is huge in terms of both dollars and societal impact. There is clear motivation for chip designers and manufacturers to make their devices as energy efficient as possible while still meeting the key requirements for each application. Low power consumption can be an important product differentiator, especially for devices that run on batteries. Historically, most of the work on improving efficiency and lowering power requirements has focused on portable consumer devices. Users want as much functionality as they can get while having reasonable battery life, and so the power performance tradeoffs made both during the design process and on the fly during device operation are critical.

Heat dissipation is also a major challenge for small form factors such as smartphones, tablets, laptops and wearable technology. Consumers must be able to hold these devices without discomfort, but spreading out the heat to avoid hot spots adds cost and bulk to the products. The only solution is to manage power consumption at the source. It is worth noting that small devices do not necessarily contain small chips. While many Internet of Things (IoT) applications are relatively simple, some of the largest and most complex SoCs in the world are used in smartphones. Autonomous vehicles are not exactly small applications, but they are still consumer devices and also require sophisticated SoCs, sensors and other electronic components.

Larger systems, from desktops to servers, offer more options for heat dissipation and thermal management. Advanced chip packaging, large heat sinks, fans and even liquid cooling are feasible for many designs, but they add significant cost. Ultra-low power is not required but power consumption must be managed. Studies have shown that the cost to power a data center server over its useful lifetime exceeds the initial outlay for the hardware itself. There is clear financial motivation to make the SoCs in these systems energy efficient as well. Many buyers also want to reduce their carbon footprint whenever possible, whether due to personal concern over global climate change or to “green laws” that limit power consumption for data centers and even individual classes of machines. New applications, especially those powered by artificial intelligence (AI) and machine learning (ML), constantly demand more power. A better energy aware design process is required.



PrimePower RTL provides more accurate analysis built on embedded RTL Architect physical and timing aware predictive technology and signoff PrimePower engines. Once the SoC or subsystem is ready for emulation, ZeBu Empower is used to profile software workloads to identify windows of high interest (such as peak power and regions of high average power) that can then be used for more detailed analysis in PrimePower RTL. Only ZeBu Empower has the power emulation capacity and performance to handle full SoC software workloads with billions of cycles.

As the design goes into implementation, further refinement of the activity windows drives implementation in Fusion Compiler. Its

- Power Intent Consistency Checks: Syntax and semantic checks on UPF that help validate the consistency of UPF prior to implementation
- Architectural Checks: Global checks at RTL for signals violating power architecture rules
- Structural and Power and Ground (PG) Checks: Validation of insertion and connection of isolation cells, power switches, level shifters, retention registers and always-on cells throughout the implementation flow
- Functional Checks: Checks for the correct functionality of isolation cells and power switches

These checks can be run at any stage of design from RTL to the final layout netlist. Additionally, these checks can be invoked directly from Fusion Compiler at various stages of the RTL-to-GDSII flow to ensure that the power intent of the design is preserved during implementation. The VC SpyGlass™ RTL Static Signoff platform also reads UPF so that checks for clock domain crossing (CDC) and reset domain crossing (RDC) instances are power aware. The same is true for the logical equivalence checking (LEC) performed by Formality® and the analysis performed by VC Formal™. Both the ZeBu emulation system and the HAPS® prototyping solution also take UPF into account. All these tools and technologies share Verdi as a unified debug platform, with many power aware debug features available. The result is a seamless flow from power intent specification through all phases of functional verification.

Many SoC applications require minimal power consumption to extend battery life or careful power management to meet regulatory and market requirements. However, the overall PPA goals cannot be comprised by focusing just on power. In response, the chip industry has developed an end-to-end design flow for energy efficiency at every stage. Early architectural exploration of power options must be followed by power aware implementation and verification, linked by a common UPF description of power intent as well as unified debug. The holistic Synopsys end-to-end low power solution is the industry's most mature and most advanced way to achieve end-to-end energy efficiency in SoC development. Every project for every application should have these capabilities.

02/17/22.CS829506549-A Holistic Approach to Energy-Efficient System-on-Chip (SoC) Design-WP.

Pub: Feb. 2022