

Overview

Stress engineering is mandatory to meet the performance targets of leading-edge CMOS technology and is now extending to strained SiGe channels and hybrid orientation of NMOS and PMOS devices. This involves a large number of possible device configurations for exploring and optimizing MOSFET performance, which can only be investigated efficiently with the help of TCAD. Yet, the complexity of stress effects, ranging from the impact of stress on process simulation to 3D effects and drain current enhancement in the quasi-ballistic transport regime of nanoscale transistors, makes TCAD simulation a challenging task.

Synopsys TCAD Services offers a range of services to address device optimization and process engineering offer many degrees of freedom to optimize device

DZ Vā` T\ValR_UQrj` fāc iZ` Zf`_ cēV` U iōj deRj] XcRaYZtō cV_eReZ _dl

aVdWc^ R_TVōh ZYZ_āVōXZyV_āVgZVōh_Z_U` hZē4 25ōRj] h dō
WcōR_āVWZV_ēRddVdd^ V_ēō VāVāUZWV_ēō` _VXf cReZ _dlōRdō
Zj]f deRe/UāZ_ōZxf cVō tōh YZYāY` h dōRāj aZRjō5ō` VTYR_ZRjō
deVddāiZ` f]ReZ`_tōR_UāZ_ōZxf cVō tōh YVcVāVōVWWTō VāYZYō
deVddōR_Uōbf RdZ SRj]ZēZ_āR_da` cēō_āVō_UtdRe`ōXRZ_āiō
UV^`_deReVUōZ f cōV_ēōdeVddōV_XZ_VVcZ_XōRaac RTYVdōVj]ō_ōRō
jRcXVō_f^ SVcō VāVddōV TY_Zbf Vd_āVēYāiē āQj` ^`_ē` b` h

_ōRō
^ Re/cRj]dZ



Figure 1: Stress component normal to the gate interface in the Si body of the MOSFET.

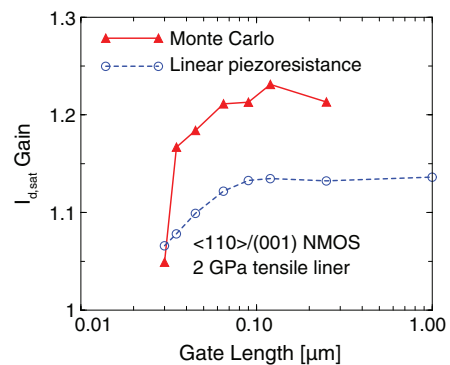


Figure 2: Scaling of the stress-induced on-current gain.

