## Overview

Stress engineering is mandatory to meet the performance targets of leading-edge CMOS technology and is now extending to strained SiGe channels and hybrid orientation of NMOS and PMOS devices. This involves a large number of possible device configurations for exploring and optimizing MOSFET performance, which can only be investigated efficiently with the help of TCAD. Yet, the complexity of stress effects, ranging from the impact of stress on process simulation to 3D effects and drain current enhancement in the quasi-ballistic transport regime of nanoscale transistors, makes TCAD simulation a challenging task.

Synopsys TCAD Services offers a range of services to address device optimization and process inre˚ n ® engineering offer many degrees of freedom to optimize device

Figure 1: Stress component normal to the gate interface in the Si body of the MOSFET.

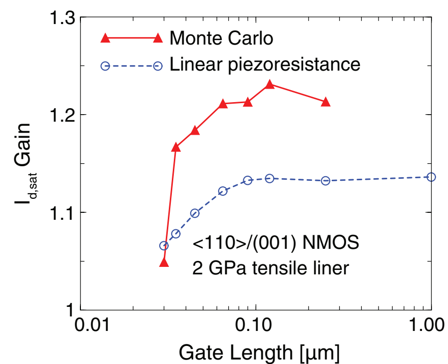


Figure 2: Scaling of the stress-induced on-current gain.

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