Proteus WorkBench (PWB) is Synopsys' powerful cockpit tool for development and optimization of Proteus-based mask synthesis solutions. It is based on an effective hierarchical GDSII/OASIS layout visualization and analysis engine, providing a comprehensive environment for lithography simulation, compact model building, full-chip optical proximity correction (OPC) recipe tuning, layout verification, and mask synthesis flow development.

PWB offers an easy to use platform with access to a wide-ranging set of tools, enabling fast calibration of accurate models, supporting the optimization of highly efficient Proteus recipes for deployment in OPC and verification.

As state-of-the-art lithography exposure tools are operated at their physical resolution limit, new mask and process technologies are being deployed to further shrink features relevant for pattering at advanced technology nodes. Consequently, the requirements for optical proximity correction (OPC) and verification become increasingly challenging. Compact models calibrated against large experimental datasets need to accurately reflect the lithographic performance for a wide range of designs, and correction recipes

- Enable high-speed layout visualization and lithographic performance analysis
- Save engineering time through automation
- Optimize parameters for unmatched full chip OPC and RET performance
- Interface with Synopsys' rigorous lithography process simulation suite, Sentaurus Lithography (S-Litho)