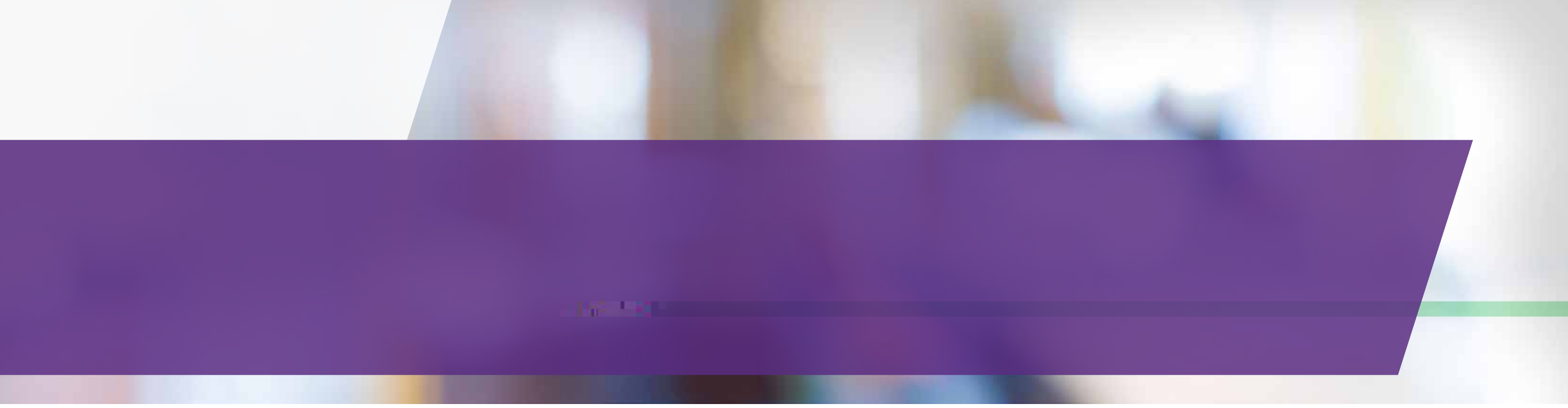

Overview

Nanometer node yield issues are dominated by design-process-test interactions, mandating cross-domain analyses to mitigate these issues rapidly. Yield Explorer brings yield relevant data from diverse sources such as the physical design flow, wafer manufacturing, and wafer and chip level testing into a single data bank. With the widest possible range of data at their disposal, users achieve unsurpassed clarity in root cause analysis when faced with systematic yield limiters. Yield Explorer achieves this with an order of magnitude advantage in analysis speed in the most complex of use cases—for example, 10X faster volume diagnostics analysis of ATPG output.

This significant analysis capability and speed advantage sets Yield Explorer in a class apart fr whapart fr wh36(Trse iou)9(om le)]me (a6(esplor)enaal,ID CID JETfirMC timnaltruD 6BDC E

Design At the Core of All Activities

A built-in layout viewer makes it easy to correlate any yield relevant information to physical design, e.g. failing cells to DRC flags or lithographic marginalities (Figure 1).

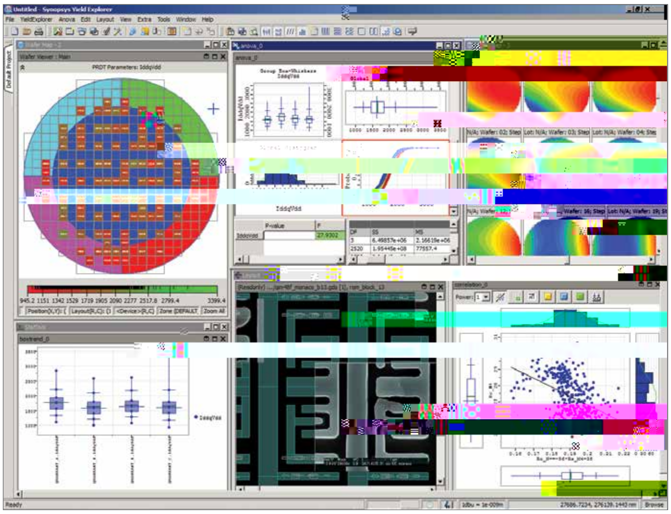
Untitled - Synopsys Yield Explorer
File YieldExplorer Anova Edit Layout View Extra Tools Window Help
Wafer Viewer : Main
anova_0
correlation_0
Ready

Figure 1: The versatile Yield Explorer client simultaneously manages a variety of yield data

Customization and end-User Control

Analysis routines are easily automated, and the application can be rapidly extended using built-in industry-standard scripting.

Rapid and Secure Data Access

Mobile and geographically distributed workforces can easily and actively participate in data-driven decision making.

Yield Explorer Benefits

- Improved turnaround time to find design, test and production problems (from weeks to hours)
- Quality of results (high accuracy of failure analysis candidate identification)
- Easy customization of recipes for each customers’ unique requirements (editable in Tcl scripting environment)
-

Typical Yield Explorer Use Case

One of the key decisions in solving yield issues on early silicon lots is to separate the random yield loss from systematic yield loss. Most often, random yield loss is controlled by fab defectivity and is handed over to the fab to rectify.

Systematic issues, however, need careful analysis by product and test engineers to understand the root cause of the failures leading