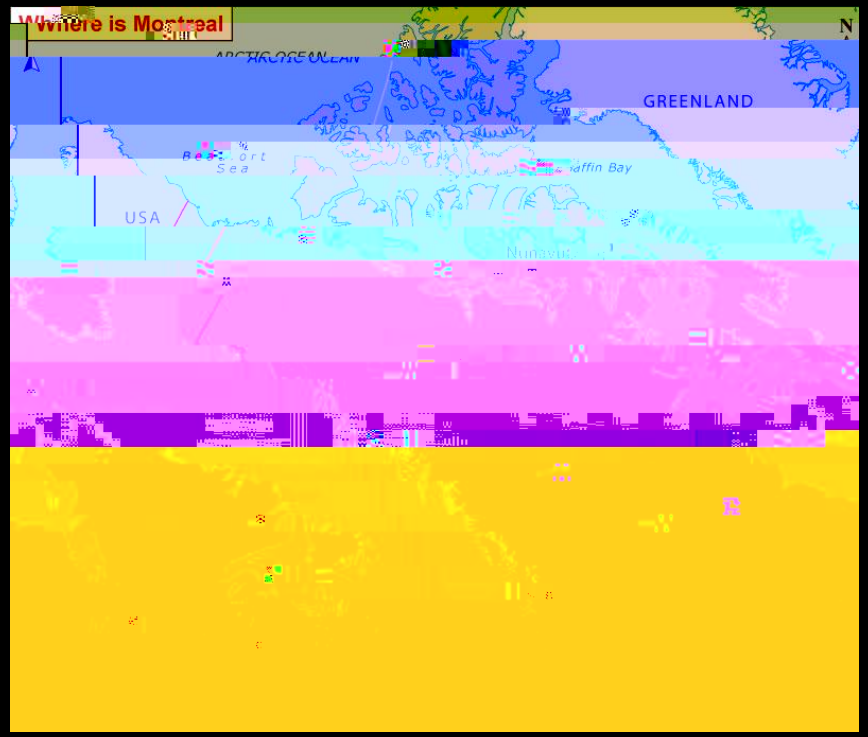


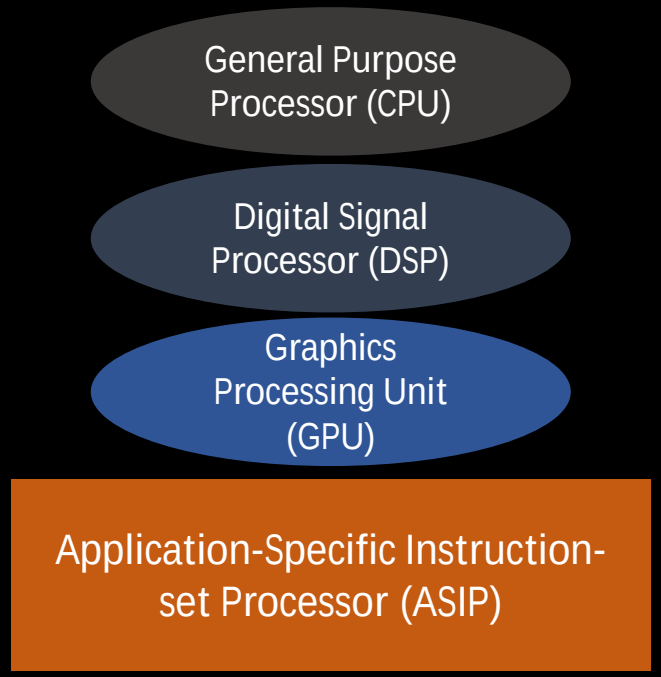
https://www.whereig.com/

Å S. Vakili, J.M.P. Langlois and G. Bois, “Enhanced

Å H. Bendaoudi, F. Cheriet, H. Ben Tahar and J.M.P. Langlois, “A

- Å Functional units
- Å Memory hierarchy
- Å Performance metrics
- Å Pipelining and parallel processing
- Å Instruction set architecture
- Å Microarchitecture
- Å Compilers

More flexible



- INF8505 : Embedded Configurable Processors
  An advanced computer architecture course

- Senior undergraduate (European M2) / graduate course
- Computer and Electrical Engineering students
- 20-30 students per year
- Taught mostly in French, but English-friendly
- Taught by me or my grad students

- 3-credit course = 135 hours of student work:
  - 33 hours of class discussions
  - 25 hours reading research papers and preparing reports
  - 18 in-lab + 9 out-

- Microprocessor design
- ASIPs and configurable processors
- Microprocessor performance metrics
- High performance processors, superscalar, VLIW, etc.
- Architecture (Processor) Description Languages :
  - MIMOLA, LISA, nML
- ASIP applications : cryptography, image processing, general DSP, neural networks
- Loop analysis : how much can you really accelerate your application ?
- The compilation problem and retargetable processors
- Automated ASIP configuration

Å 2008

Å Objectives :
Å

Ming-Zher Poh; Swenson, N.C.; Picard, R.W., "A

https://www.researchgate.net/profile/Stephen-Dicarlo

- Students must read one (or portions of one) paper and hand-in a one-page report every week
- The paper is then discussed in class and serves as a basis to cover that week's subject matter
- Counts for 20% of final mark
- Sample papers :
  - S. Radhakrishnan et al. "Customization of application specific heterogeneous multi-pipeline processors," DATE 2006.
  - Q. Jinguo et al. "Fine-grained analysis and design of ASIP instruction set for application of encryption," ICNC 2012.
  - A. Gupta et al. "Accelerating SVM on Ultra Low Power ASIP for High Throughput Streaming Applications," in IEEE VLSI 2015.
  - Y. Xin et al. "An Application Specific Instruction Set Processor (ASIP) for Adaptive Filters in Neural Prosthetics," in IEEE/ACM Transactions on Computational Biology and Bioinformatics 2015.
  - I.

- Remember Amdahl's law
- The chosen algorithm should not be too complex – should be clearly representable with a half-page datapath
- The application must benefit from acceleration :
  - High throughput more than low latency
- There should be a balance between computation effort and data access needs
- Avoid algorithms requiring lots of divisions and transcendental functions (unless that is the goal of the project)
- Avoid floating point computation (unless that is the goal of the project)

- Students are very satisfied with their learning outcomes
  - Enjoy reading, commenting and discussing research papers
  - Enjoy performing the project, although it is a lot of work
  - Enjoy practicing the regular research steps
    - Literature : what is the problem
    - Objectives : what we want to about the problem
    - Proposals : what are our ideas
    - Results : what we achieved
    - Compare : how did we do

- Remember Amdahl’s law
- The chosen algorithm should not be too complex – should be clearly representable with a half-page datapath
- The application must benefit from acceleration :
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- Students are very satisfied with their learning outcomes
  -

prof. Michael Peshkin, NWU, Illinois USA

- The course INF8505 – Embedded Configurable Processors – is a three-credit, 135-hour graduate computer architecture course that has been running in Polytechnique Montréal since 2008. It is also available as an elective to senior Electrical and Computer Engineering undergraduates. The course focuses on Application Specific Instruction set Processor (ASIP) design, and its main topics are custom datapath and custom memory hierarchy design, processor description languages, retargetable compilers, and processor performance metrics. It exploits high throughput applications such as deep learning, image processing and cryptography to demonstrate the ASIP's potential. From its beginning, the course has been taught in a flipped-classroom style where students are assigned one research paper every week for which they must produce a one-page report. The paper is then discussed in class and the instructor weaves the course topics with the paper's main contributions. A major 52-hour course project is anchored in laboratory exercises. Two-student teams use Synopsys' ASIP Designer to design and simulate an ASIP tailored to an application of their choice, then submit a project report as a 4- or 6-page research paper. To date, there are almost 250 course alumni and half a dozen project report papers have been presented in international conferences.