

LPDDR4

0

Ma G
DDR IP,
S

LPDDR4

0

9

1

A

0

/09/

0/

55-

5-

5-

5-

5-

5-

5-

5-

5-

5-

5-

5-

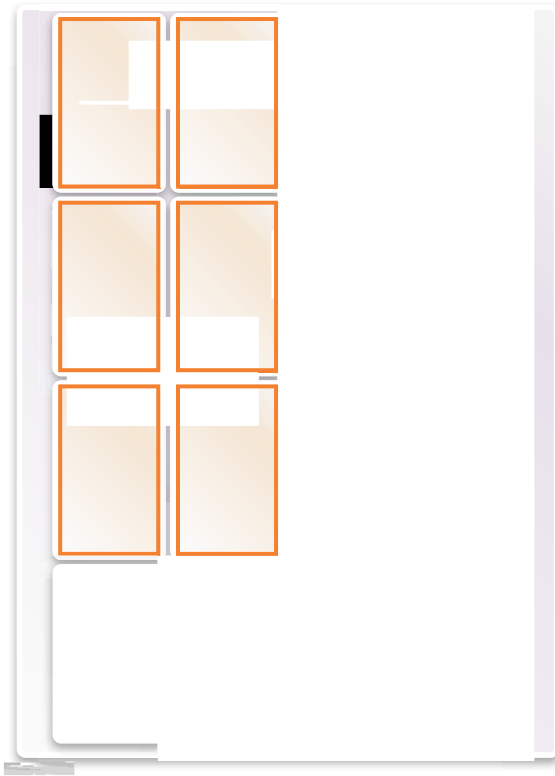
5-

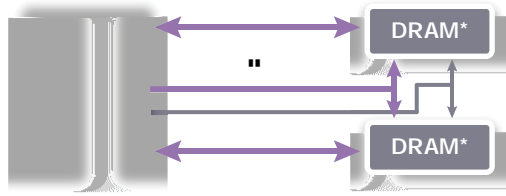
5-

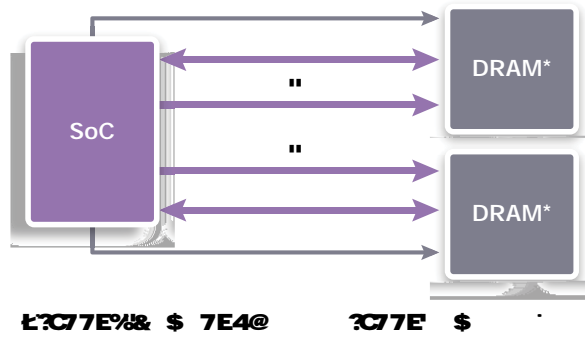
5-

5-

5-



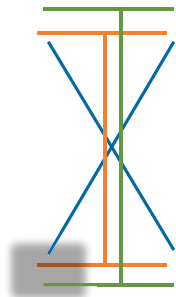
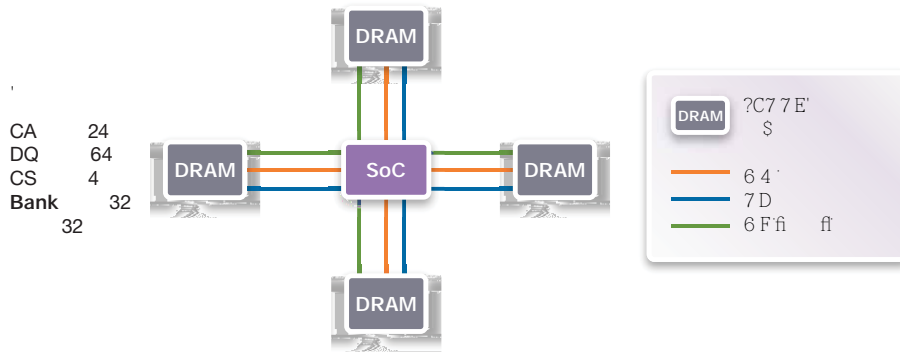


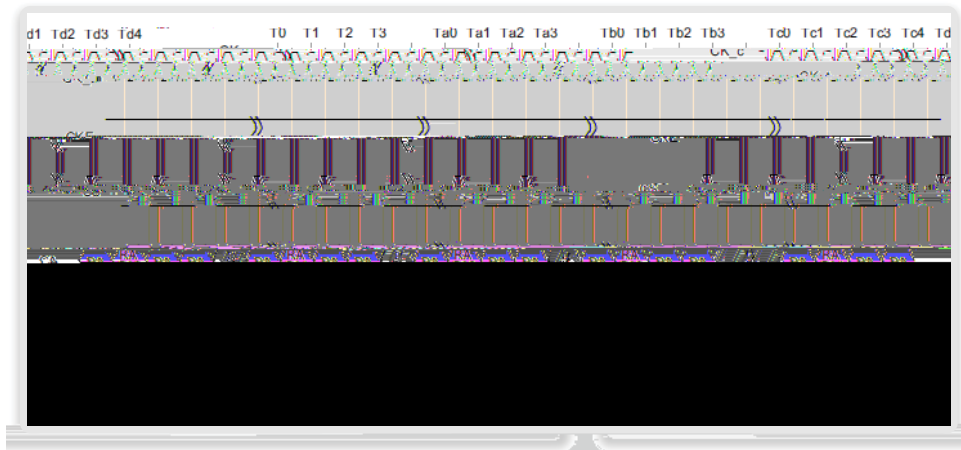


/ CA

*

2 4





%& h5K hFF8

A / A0 -1 0

/ A

-1

-1

A

00%

00 00

并行



